GDA 9803 - CORRELATOR BOARD FOR CALTECH

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SEE THE HEIRARCHY MAP ON p4 FOR THE MAP OF PAGE NUMBERS TO HIERARCHICAL BLOCKS.

Revision C.1
The H? references in the folder shapes indicate the hierarchy block number associated with the folder name. The p? references next to the folder shapes indicate the page number of the schematic (in physical mode).
THE CORRELATOR BOARD JTAG CHAIN

THERE ARE THREE OPTIONS FOR JTAG CHAINS. THE FIRST OPTION IS USED FOR BOARD DEBUGGING AND INITIAL BRING-UP OF THE BOARDS. USING THE EXTERNAL HEADER AND BY SHORTING PINS 1 AND 2 OF THE JUMPER BLOCK, A SINGLE DEVICE JTAG CHAIN IS FORMED WITH THE SYSTEM CONTROLLER. IN THE SECOND OPTION, IT IS ASSUMED THAT THE SYSTEM CONTROLLER IS TRI-STATEd, OR AT LEAST, IS NOT DRIVING JTAG_SEL LOW AND THAT JUMPER PINS 2 AND 3 ARE SHORTED. THIS FORMS A 12 DEVICE JTAG CHAIN.

IN THE THIRD OPTION, THE MULTIPLEXER IS USED TO CONTROL THE CORRELATOR FPGA AND EPROM JTAG CHAIN. THE 10 CORRELATOR FPGAS (0 TO 9) ARE CONSECUTIVELY LINKED IN THE JTAG CHAIN FOLLOWED BY THE SYSTEM CONTROLLER EPROM. WHEN THE SYSTEM CONTROLLER IS CONFIGURED, THE SYSTEM CONTROLLER CAN DRIVE JTAG_SEL LOW AND THEN THE JTAG SIGNALS FOR THE CORRELATOR CHAIN WILL ORIGINATE FROM THE SYSTEM CONTROLLER. THIS OPTION CAN BE USED FOR CORRELATOR FPGA CONFIGURATION INSTEAD OF PASSIVE SERIAL CONFIGURATION AND IT CAN BE USED TO REPROGRAM THE EPROM. THE JTAG CHAIN CAN ALSO BE USED FOR BOUNDARY SCAN TESTS ORIGINATING FROM THE JTAG HEADER OR THE PCI INTERFACE. A JAM PLAYER LOCATED IN THE HOST COMPUTER OR IN THE BOARD DSP CAN BE USED FOR CONTROLLING THIS JTAG INTERFACE.

RESISTOR PADS ARE AVAILABLE TO SHORT TDI AND TDO ON THE 10 FPGAS. THIS ALLOWS A REDUCED NUMBER OF FPGAS TO BE LOADED WHILE STILL COMPLETING THE JTAG CHAIN.
GND = POWER SUPPLY COMMON THROUGH THE CPCI BACKPLANE

GROUND AND CHASSIS GROUND ARE TIED TOGETHER AS OFTEN AS POSSIBLE (EVERY INCH) WITH A CAPACITOR.

VCC_INT IS REQUIRED ONLY BY THE CORRELATOR FPGA AND VTTL IS REQUIRED ONLY BY SOME OF THE CONTROL CIRCUITS AND THE DELAY CHIP. PLACES WHERE VTTL OR VCC_INT ARE NOT REQUIRED SHOULD BE FLOODED AS GND AND TIED TO GND WITH VIAS.

TELESCOPE DATA ROUTING FOR A 5 BASE LINE CROSS-CORRELATOR

NOTE: DASHED LINE INDICATES DATA PATH ROUTED FOR USE IN SINGLE TELESCOPE AUTO-CORRELATOR AND SINGLE BASELINE CROSS-CORRELATOR
NOTES:

1. The pull-up on CF_PS_CONFIG causes the correlator FPGAs to perform a power-on-reset and enter configuration mode on power-up.

2. The last buffers in these devices are available for rework if required.

ATTEMPT TO PLACE A DECOUPLING CAP ON EVERY VCC PIN
RIN = 7.5MHz to 17.5MHz
FIN = 7.5MHz to 35MHz
FOUT = 30MHz to 140MHz
HFOUT = 480MHz to 1120MHz

PLACEMENT OF THE TERMINATION RESISTOR PACKS IS CRITICAL IN THE HIGH FREQUENCY PATHS.


PLL DEFAULT CONTROL SETTINGS ARE
PLL(3..0) = (1, 0, 1, 0), P = 2, N = 8, WITH A 10.625MHz REFERENCE INPUT; HFOUT = 1GHz, FOUT = 125MHz.

SY89421: For the TTL inputs, I_IL = -0.3mA, I_IH = 100uA. So Rpu < 1.2V/I_IH = 12k, and Rpd < 0.5V/I_IL = 1k6.

THE INVERSION BETWEEN THE LEVEL11 OUTPUTS AND THE NET NAMES IS DELIBERATE. DO NOT CHANGE IT.
ATTEMPT TO PLACE A DECOUPLING CAP ON EVERY VCC PIN

PLACE THE TERMINATION RESISTOR PACKAGE CLOSE TO THE MPC949

PULL-UP ON FANOUT_OE# TRISTATES THE LATCH OUTPUTS. THE POWER-UP STATE OF THE FANOUT CHIP IS THEN DETERMINED BY THE STUFF-RESISTORS. THE SYSTEM CONTROLLER CAN CHANGE THE FANOUT CONTROL SETTING BY LATCHING THE NEW CONTROL VALUES AND ENABLING THE LATCH OUTPUTS.

PLACE PADS FOR, BUT DO NOT STUFF, RESISTORS MARKED WITH A BOX.

ADDITIONAL DECOUPLING. PLACE ONLY IF SPACE PERMITS (DO NOT STUFF)

PULL-UP ON FANOUT_OE# TRISTATES THE LATCH OUTPUTS. THE POWER-UP STATE OF THE FANOUT CHIP IS THEN DETERMINED BY THE STUFF-RESISTORS. THE SYSTEM CONTROLLER CAN CHANGE THE FANOUT CONTROL SETTING BY LATCHING THE NEW CONTROL VALUES AND ENABLING THE LATCH OUTPUTS.

POWER-UP FANOUT CHIP STATE:

- FANOUT6 = MR/OE# LOW  Output clocks are enabled (option for HIGH = outputs disabled)
- FANOUT5 = TCLK_SEL LOW  33MHz selected
- FANOUT4 = PCLK_SEL HIGH  PECL clock source (option for LOW = TTL clock input)
- FANOUT1 = DSELB HIGH  Output = Input/2
- FANOUT0 = DSELA HIGH  Output = Input/2

These settings produce nominal 62.5MHz clocks for CLK_LVDS_TX[3..0], CLK_FANOUT, and CLK_CORL_A[9..0], and 125MHz clocks for CLK_CORL_B[9..0].
CLK_CORL_A[9..0] AND CLK_CORL_B[9..0] ARE ROUTED TO THE 10 CORRELATOR FPGAS. EITHER CLOCK CAN BE CONFIGURED AS CLKx1 OR CLKx2 USING THE MPC949 CONTROLS.

ALL RESISTORS SHOWN ON THIS PAGE ARE SOURCE TERMINATIONS. AS SUCH, THEY MUST BE LOCATED ON THE SAME LAYER AS THE MPC949 AND BE PLACED AS CLOSE TO THE CHIP AS POSSIBLE. (Rout FOR THE MPC949 IS ABOUT 7-OhMS IN THE HIGH OR LOW STATE).
+12V is used by the reference for the monitor DAC. -12V is not used.

ALtera AN-41 shows the required PCI pins. Pin directions differ between master and target implementations. Pin directions shown are for a target implementation.

Only PCI_INTA# is routed, as this is a single function device.

Supply decoupling is shown on the power distribution page.

All cPCI backplane connector shields are tied to ground (power supply common) not chassis ground.
STUFFING OPTION FOR FPGAS THAT ARE NOT LOADED. PLACE THE PADS FOR THESE TWO RESISTORS UNDER THE BGA FOOTPRINT ON THE SAME SIDE OF THE PCB AS THE FPGA. THESE RESISTORS ARE ONLY TO BE LOADED IF AN FPGA IS NOT PRESENT.

CONTROL SIGNAL INTERFACE

SEE ALTERA AN-59 AND THE BYTEBLASTER DATA SHEET FOR MORE DETAILS ON PASSIVE SERIAL CONFIGURATION. CF_PS_CONFIG#, CF_PS_DONE, AND CF_PS_STATUS# (SIGNS COMMON TO THE 10 CORRELATOR FPGAS) ARE PULLED UP WITH 1K BACK AT THE SYSTEM CONTROLLER. AN-59, FIGURE 8, PAGE 8 SHOWS THE PASSIVE SERIAL CHAIN IMPLEMENTED IN THIS SYSTEM.

PULL-DOWNS ARE REQUIRED ON THE CLOCK LINES AS THESE SIGNALS CAN BE TRISTATED. THE LVDS CLOCK IS TRISTATED WHEN THE LVDS TRANSCEIVERS ARE IN TRANSMIT MODE, WHILE THE CORL_CLKS ARE TRISTATED WHEN THE MPC049 IS TRISTATED (POWER SAVE MODE).
CORRELATOR FPGA NUMBER: 1
CORRELATOR FPGA NUMBER: 1

CF_RDY# and CF_CORL_DONE# are pulled low or tri-stated by the Correlator FPGA. Pull-ups for these signals are located at the system controller.

See ALTERA AN-59 and the ByteBlaster data sheet for more details on passive serial configuration. CF_PS_CONFIG#, CF_PS_DONE, and CF_PS_STATUS# (signals common to the 10 Correlator FPGAs) are pulled up with 1K back at the system controller. AN-59, Figure 8, Page 8 shows the passive serial chain implemented in this system.

Pull-downs are required on the clock lines as these signals can be tri-stated. The LVDS clock is tri-stated when the LVDS transceivers are in transmit mode, while the Correlator clocks are tri-stated (Power Save Mode).

Stuffing option for FPGAs that are not loaded. Place the pads for these two resistors under the BGA footprint on the same side of the PCB as the FPGA. These resistors are only to be loaded if an FPGA is not present.

CF_SEL# and CF_CORL_MODE# are pulsed low or tri-stated by the Correlator FPGA, pull-ups for these signals are located at the system controller.

This surface mount LED lights when the FPGA is configured (passive serial or JTAG configuration).

STUFFING OPTION FOR FPGAS THAT ARE NOT LOADED. PLACE THE PADS FOR THESE TWO RESISTORS UNDER THE BGA FOOTPRINT ON THE SAME SIDE OF THE PCB AS THE FPGA. THESE RESISTORS ARE ONLY TO BE LOADED IF AN FPGA IS NOT PRESENT.
CORRELATOR FPGA NUMBER: 2
STUFFING OPTION FOR FPGAS THAT ARE NOT LOADED.
PLACE THE PADS FOR THESE TWO RESISTORS UNDER THE
BGA FOOTPRINT ON THE SAME SIDE OF THE PCB AS THE
FPGA. THESE RESISTORS ARE ONLY TO BE LOADED IF AN
FPGA IS NOT PRESENT.

A (1K PULL-UP IS
RECOMMENDED ON EACH
TDI IN THE JTAG CHAIN -
ALTERA HOTLINE)

SEE ALTERA AN-59 AND THE BYTEBLASTER DATA SHEET
FOR MORE DETAILS ON PASSIVE SERIAL CONFIGURATION.
CF_PS_CONFIG, CF_PS_DONE, AND CF_PS_STATUS
(SIGNALS COMMON TO THE 10 CORRELATOR FPGAS) ARE
PULLED UP WITH 1K BACK AT THE SYSTEM CONTROLLER.
AN-59, FIGURE 8, PAGE 8 SHOWS THE PASSIVE SERIAL
CHAIN IMPLEMENTED IN THIS SYSTEM.

PULL-DOWNS ARE REQUIRED ON THE
CLOCK LINES AS THESE SIGNALS CAN
BE TRISTATED. THE LVDS CLOCK IS
TRISTATED WHEN THE LVDS
TRANSCEIVERS ARE IN TRANSMIT
MODE, WHILE THE CORRELATE CLKS ARE
TRISTATED (POWER SAVE MODE).
CORRELATOR FPGA NUMBER: 3
CORRELATOR FPGA NUMBER: 3
THE FPGA IS CONFIGURED (PASSIVE SERIAL OR JTAG CONFIGURATION).

PLACE THE PADS FOR THESE TWO RESISTORS UNDER THE BGA FOOTPRINT ON THE SAME SIDE OF THE PCB AS THE FPGA. THESE RESISTORS ARE ONLY TO BE LOADED IF AN FPGA IS NOT PRESENT.

PULL-DOWNS ARE REQUIRED ON THE CLOCK LINES AS THESE SIGNALS CAN BE TRISTATED. THE LVDS CLOCK IS TRISTATED WHEN THE LVDS TRANSEIVERS ARE IN TRANSMIT MODE, WHILE THE CORR_CLKS ARE TRISTATED WHEN THE MPC949 IS TRISTATED (POWER SAVE MODE).

SEE ALTERA AN-59 AND THE BYTEBLASTER DATA SHEET FOR MORE DETAILS ON PASSIVE SERIAL CONFIGURATION. CF_PS_CONFIG#, CF_PS_DONE, AND CF_PS_STATUS# (SIGNALS COMMON TO THE 10 CORRELATOR FPGAs) ARE PULLED UP WITH 1K BACK AT THE SYSTEM CONTROLLER. AN-59, FIGURE 8, PAGE 8 SHOWS THE PASSIVE SERIAL CHAIN IMPLEMENTED IN THIS SYSTEM.
CORRELATOR FPGA NUMBER: 4
CORRELATOR FPGA NUMBER: 4

SEE ALTEGRA AN-59 AND THE BYTEBLASTER DATA SHEET FOR MORE DETAILS ON PASSIVE SERIAL CONFIGURATION. CF_PS_CONFIG, CF_PS_DONE, AND CF_PS_STATUS (SIGNALS COMMON TO THE 10 CORRELATOR FPGAS) ARE PULLED UP WITH 1K BACK AT THE SYSTEM CONTROLLER. AN-59, FIGURE 8, PAGE 8 SHOWS THE PASSIVE SERIAL CHAIN IMPLEMENTED IN THIS SYSTEM.

PULL-DOWNS ARE REQUIRED ON THE CLOCK LINES AS THESE SIGNALS CAN BE TRISTATED. THE LVDS CLOCK IS TRISTATED WHEN THE LVDS TRANSCEIVERS ARE IN TRANSMIT MODE, WHILE THE CORL CLKS ARE TRISTATED WHEN THE MPC949 IS TRISTATED (POWER SAVE MODE).

STUFFING OPTION FOR FPGAS THAT ARE NOT LOADED. PLACE THE PADS FOR THESE TWO RESISTORS UNDER THE BGA FOOTPRINT ON THE SAME SIDE OF THE PCB AS THE FPGA. THESE RESISTORS ARE ONLY TO BE LOADED IF AN FPGA IS NOT PRESENT.
CORRELATOR FPGA NUMBER: 5

STUFFING OPTION FOR FPGAS THAT ARE NOT LOADED.
PLACE THE PADS FOR THESE TWO RESISTORS UNDER THE BGA FOOTPRINT ON THE SAME SIDE OF THE PCB AS THE FPGA. THESE RESISTORS ARE ONLY TO BE LOADED IF AN FPGA IS NOT PRESENT.

SEE ALTERA AN-59 AND THE BYTEBLASTER DATA SHEET FOR MORE DETAILS ON PASSIVE SERIAL CONFIGURATION.

PULL-DOWNS ARE REQUIRED ON THE CLOCK LINES AS THESE SIGNALS CAN BE TRISTATED. THE LVDS CLOCK IS TRISTATED WHEN THE LVDS TRANSEIVER IN TRANSIT MODE, WHILE THE CORL_CLKS ARE TRISTATED WHEN THE MPC949 IS TRISTATED (POWER SAVE MODE).

SEE ALTERNATIVE AN-59 ATTACHMENT AND THE BYTEBLASTER DATA SHEET FOR MORE DETAILS ON PASSIVE SERIAL CONFIGURATION. CF_PS_CONFIG#, CF_PS_DONE, AND CF_PS_STATUS# (SIGNALS COMMON TO THE 10 CORRELATOR FPGAS) ARE PULLED UP WITH 1K BACK AT THE SYSTEM CONTROLLER. AN-59, FIGURE 8, PAGE 8 SHOWS THE PASSIVE SERIAL CHAIN IMPLEMENTED IN THIS SYSTEM.
CORRELATOR FPGA NUMBER: 6

TELESCOPE DATA BUS E

TELESCOPE DATA BUS G

TELESCOPE DATA BUS F

FPGA_CORL
CORRELATOR FPGA NUMBER: 6

THIS SURFACE MOUNT LED LIGHTS WHEN THE FPGA IS CONFIGURED (PASSIVE SERIAL OR JTAG CONFIGURATION).

PLACE THE PADS FOR THESE TWO RESISTORS UNDER THE BGA FOOTPRINT ON THE SAME SIDE OF THE PCB AS THE FPGA. THESE RESISTORS ARE ONLY TO BE LOADED IF AN FPGA IS NOT PRESENT.

STUFFING OPTION FOR FPGAS THAT ARE NOT LOADED. PLACE THE PADS FOR THESE TWO RESISTORS UNDER THE BGA FOOTPRINT ON THE SAME SIDE OF THE PCB AS THE FPGA. THESE RESISTORS ARE ONLY TO BE LOADED IF AN FPGA IS NOT PRESENT.

SEE ALTERA AN-59 AND THE BYTEBLASTER DATA SHEET FOR MORE DETAILS ON PASSIVE SERIAL CONFIGURATION. CF_PS_CONFIG#, CF_PS_DONE, AND CF_PS_STATUS# (SIGNS COMMON TO THE 10 CORRELATOR FPGAS) ARE PULLED UP WITH 1K BACK AT THE SYSTEM CONTROLLER. AN-59, FIGURE 8, PAGE 8 SHOWS THE PASSIVE SERIAL CHAIN IMPLEMENTED IN THIS SYSTEM.

PULL-DOWNS ARE REQUIRED ON THE CLOCK LINES AS THESE SIGNALS CAN BE TRISTATED. THE LVDS CLOCK IS TRISTATED WHEN THE LVDS TRANSEIVERS ARE IN TRANSMIT MODE, WHILE THE CORL CLKS ARE TRISTATED WHEN THE MP6499 IS TRISTATED (POWER SAVE MODE).

9803.dsn/Correlator FPGA Part C-Contr/Correlator FPGA Part C-Control

GDA Technologies Inc.,
2071, Junction Avenue,
San Jose - 95131.
Tel: (408) 432-3090 
Fax: (408) 432-3091 
www.gdatech.com
CORRELATOR FPGA NUMBER: 7

Signals to Part B

CF_TDA0
CF_TDB0
CF_TDC0
CF_TDD0

CF_TDA1
CF_TDB1
CF_TDC1
CF_TDD1

CF_TDA2
CF_TDB2
CF_TDC2
CF_TDD2

CF_TDA3
CF_TDB3
CF_TDC3
CF_TDD3

CF_TDA4
CF_TDB4
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CF_TDC30
CF_TDD30

CF_TDA31
CF_TDB31
CF_TDC31
CF_TDD31
CORRELATOR FPGA NUMBER: 7

**Diagram Description:**

- **CF_RDY# and CF_CORL_DONE#** are pulled low or tri-stated by the Correlator FPGA. Pull-ups for these signals are located at the system controller.

- **CF_ADDR[11..0]**: Address lines for configuration.

- **MSEL[1..0] = 0** - Passive Serial Configuration Scheme

- **CLK_CORL_A** and **CLK_CORL_B**: Clock lines for correlator.

- **CLK_LVDS_RX** and **CLK_33MHZ**: Clock lines for LVDS transceivers.

- **CF_PS_CONFIG#**, **CF_PS_DONE**, and **CF_PS_STATUS#**: Signals common to the 10 Correlator FPGAs are pulled up with 1K back at the system controller. AN-59, Figure 8, Page 8 shows the Passive Serial Chain implemented in this system.

- **Pull-downs are required on the clock lines as these signals can be tri-stated.** The LVDS clock is tri-stated when the LVDS transceivers are in transmit mode, while the Corl clocks are tri-stated (power save mode).

- **See ALTERA AN-59 and the ByteBlaster data sheet for more details on Passive Serial Configuration.**

**Note:**

- The diagram shows the control signal interface and the placement of various signals and components.

**Correlator FPGA Part C-Control/Correlator FPGA Part C-Control**

**Customer: GD Technologies Inc.**

- Main Address: 2071, Junction Avenue, San Jose, 95131
- Website: www.gdatech.com

**Contact Information:**

- Tel: (408) 432-3090
- Fax: (408) 432-3091

**Document:**

- Title: Correlator FPGA Part C-Control
- Document Number: GD9803
- Revision: 2.1
- Date: Thursday, June 06, 2002
CORRELATOR FPGA NUMBER: 8
CORRELATOR FPGA NUMBER: 8

See ALTERA AN-59 and the BYTEBLASTER DATA SHEET FOR MORE DETAILS ON PASSIVE SERIAL CONFIGURATION. CF_PS_CONFIG#, CF_PS_DONE, AND CF_PS_STATUS# (SIGNALS COMMON TO THE 10 CORRELATOR FPGAS) ARE PULLED UP WITH 1K BACK AT THE SYSTEM CONTROLLER. AN-59, FIGURE 8, PAGE 8 SHOWS THE PASSIVE SERIAL CHAIN IMPLEMENTED IN THIS SYSTEM.

PULL-DOWNS ARE REQUIRED ON THE CLOCK LINES AS THESE SIGNALS CAN BE TRISTATED. THE LVDS CLOCK IS TRISTATED WHEN THE LVDS TRANSMITTERS ARE IN TRANSMIT MODE, WHILE THE CORL CLKS ARE TRISTATED WHEN THE MPC949 IS TRISTATED (POWER SAVE MODE).
CORRELATOR FPGA NUMBER: 9

CF_RDY# AND CF_CORL_DONE# ARE PULLED LOW OR TRI-STATED BY THE CORRELATOR FPGA. PULL-UPS FOR THESE SIGNALS ARE LOCATED AT THE SYSTEM CONTROLLER.

STUFFING OPTION FOR FPGAS THAT ARE NOT LOADED. PLACE THE PADS FOR THESE TWO RESISTORS UNDER THE BGA FOOTPRINT ON THE SAME SIDE OF THE PCB AS THE FPGA. THESE RESISTORS ARE ONLY TO BE LOADED IF AN FPGA IS NOT PRESENT.

CF_JTAG_TDI
CF_JTAG_TDO
CF_JTAG_TMS
CF_JTAG_TCK

(1K PULL-UP IS RECOMMENDED ON EACH TDI IN THE JTAG CHAIN - ALTERA HOTLINE)

SEE ALTERA AN-59 AND THE BYTEBLASTER DATA SHEET FOR MORE DETAILS ON PASSIVE SERIAL CONFIGURATION. CF_PS_CONFIG#, CF_PS_DONE, AND CF_PS_STATUS# (SIGNALS COMMON TO THE 10 CORRELATOR FPGAs) ARE PULLED UP WITH 1K BACK AT THE SYSTEM CONTROLLER. AN-59, FIGURE 8, PAGE 8 SHOWS THE PASSIVE SERIAL CHAIN IMPLEMENTED IN THIS SYSTEM.

PULL-DOWNS ARE REQUIRED ON THE CLOCK LINES AS THESE SIGNALS CAN BE TRISTATED. THE LVDS CLOCK IS TRISTATED WHEN THE LVDS TRANSCEIVERS ARE IN TRANSMIT MODE, WHILE THE CORL CLKS ARE TRISTATED WHEN THE MPC949 IS TRISTATED (POWER SAVE MODE).
CONNECTOR SHIELD SUPPLY DECOUPLING IS SHOWN ON THE POWER DISTRIBUTION PAGE.

ALL CPCI BACKPLANE CONNECTOR SHIELDS ARE TIED TO GROUND (POWER SUPPLY COMMON) NOT CHASSIS GROUND.
DSP ADDRESS AND DATA BUS PULL-UPS AND PULL-DOWNS

USE VCC3_CTRL IF RESISTORS ARE PLACED NEAR TO BUFFERS. USE VCC3_IO IF RESISTORS ARE PLACED AT THE END OF THE BUS.

DECOUPLING CAPACITORS FOR THE VCC_CTRL RESISTOR PACKS.

DECOUPLING FOR THE VCC_IO RESISTOR PACKS.

CORRELATOR FPGA ADDRESS AND DATA BUS PULL-UPS AND PULL-DOWNS

USE VCC3_CTRL IF RESISTORS ARE PLACED NEAR TO BUFFERS. USE VCC3_IO IF RESISTORS ARE PLACED AT THE END OF THE BUS.
DECOUPLING CAPACITORS FOR THE SYSTEM CONTROLLER FPGA VCC_INT PINS.
EVERY VCC_INT PIN SHOULD HAVE A DECOUPLING CAPACITOR CLOSE BY.

DECOUPLING CAPACITORS FOR THE SYSTEM CONTROLLER FPGA VCC_IO PINS.
EVERY VCC_IO PIN SHOULD HAVE A DECOUPLING CAPACITOR CLOSE BY.

DECOUPLING CAPACITORS FOR THE PLX-9054 PCI MASTER/TARGET.
EVERY VCC PIN SHOULD HAVE A DECOUPLING CAPACITOR CLOSE BY.

DECOUPLING CAPACITORS FOR THE DSP.
EVERY VCC PIN SHOULD HAVE A DECOUPLING CAPACITOR CLOSE BY.
DECOUPLING PROCEDURE FOR THE CORRELATOR FPGA:

SINCE THE 10 FPGA ARE LOCATED SO CLOSE, MANY OF THE DECOUPLING CAPS PLACED WILL PERFORM DECOUPLING FOR MORE THAN 1 FPGA. PLACE AS MANY OF THESE DECOUPLING CAPACITORS AS POSSIBLE. THE DENSITY OF DECOUPLING SHOULD BE UNIFORM OVER THE VCC_INT SEGMENT AND SHOULD BE SIMILAR TO THE VCC3_IO DECOUPLING.
DECOUPLING PROCEDURE FOR THE CORRELATOR FPGAS:

SINCE THE 10 FPGAS ARE LOCATED SO CLOSE, MANY OF THE DECOUPLING CAPS PLACED WILL PERFORM DECOUPLING FOR MORE THAN 1 FPGA. PLACE AS MANY OF THESE DECOUPLING CAPACITORS AS POSSIBLE. THE DENSITY OF DECOUPLING SHOULD BE UNIFORM OVER THE VCC3_IO SEGMENT AND SHOULD BE SIMILAR TO THE VCC_INT DECOUPLING.
A17 and A18 are present so that the 128K x 8-bit Am29LV010B can be upgraded to a 512K x 8-bit Am29LV040B if necessary.

PLACE ALL RESISTORS NEAR THE LOAD (RAM) END

PULL-UP/DOWNS FOR SIGNAL QUALITY TUNING. 10K PULL-UPS ARE NECESSARY TO DEASSERT CONTROL SIGNALS WHEN NO DRIVING SIGNAL IS PRESENT.

ROUTE DSP_RAM_RD#, DSP_RAM_WR# AND DSP_RAM_CS# FOR ALL THE RAM CHIPS IN A DAISY CHAIN. PUT THESE RESISTORS AT THE END OF THE CHAIN.
SYSTEM CONTROLLER CONFIGURATION EPROM

The power-on LOW-to-HIGH transition at the system controller FPGA's CONFIG# pin initiates EPROM configuration. The FPGA drives CONF_DONE LOW and this drives CS# on the EPROM LOW. The FPGA then tri-states STATUS#, and since STATUS# is connected to OE, the pull-up resistor on OE enables the EPROM. The EPC2 uses an internal oscillator to clock data to the system controller. When configuration is complete, CONF_DONE is tri-stated by the FPGA and the pull-up resistor on CS# disables the EPC2 circuit. See Altera AN-59 and the EPC data sheet for more details.

The configuration EPROM is located at the end of the JTAG chain. The system controller is first, then the 10 correlator FPGAs, then the EEPROM. The EPROM can be accessed over the JTAG chain via an external JTAG header, or via JTAG commands from the system controller. Once re-programmed, the system controller can issue a nINT_CONFIG JTAG command and the system controller EPROM will reprogram the system controller.

The correlator FPGAs are configured using a passive serial interface from the system controller or via the JTAG chain.

LOCAL CLOCK GENERATION/FANOUT

The 33MHz system clock is required at 15 devices. This clock needs to be aligned at all devices. To ease routing, two separate zero delay buffers are used; 1 for the FPGA clocks, the other for the system clocks.
ALTERA FPGA JTAG INTERFACE

The header pull-up/down resistors leave the JTAG controls in the state recommended by Altera (p25 [1] and [2]). The Altera devices have weak internal pull-ups of 100k to 200k, however, Altera recommends using external pull-ups. External pull-ups are also necessary on all TDI/TDO connections through the JTAG chain.


U89 and U91, and the pull-ups for JTAG[2..0] are powered by VCC3_IO due to their placement on the PCB.

The JTAG TCK and TMS signals fanout to 11 loads. Four output copies are required due to the arrangement of the 10 FPGAs and EPC EEPROM on the board.

The JTAG TCK and TMS signals fanout to 11 loads. Four output copies are required due to the arrangement of the 10 FPGAs and EPC EEPROM on the board.

The chosen impedances keep IOH = IOL = 16mA, and the termination impedance at 50-Ohms. See p226 Johnson and Graham for calculation details.

The JTAG TCK and TMS signals fanout to 11 loads. Four output copies are required due to the arrangement of the 10 FPGAs and EPC EEPROM on the board.

END TERMINATIONS

The chosen impedances keep IOH = IOL = 16mA, and the termination impedance at 50-Ohms. See p226 Johnson and Graham for calculation details.

The JTAG TCK and TMS signals fanout to 11 loads. Four output copies are required due to the arrangement of the 10 FPGAs and EPC EEPROM on the board.

The chosen impedances keep IOH = IOL = 16mA, and the termination impedance at 50-Ohms. See p226 Johnson and Graham for calculation details.
DECOUPLING REQUIREMENTS:

SINCE THE 4 LVDS TRANSCIEVERS ARE LOCATED VERY CLOSE TOGETHER AND ARE ON BOTH SIDES OF THE BOARD, NOT ALL DECOUPLING CAPS WILL BE NECESSARY. PLEASE PLACE AS MANY AS POSSIBLE. USE FAT TRACES TO DECOUPLING CAPS.
DECOUPLING REQUIREMENTS:

Since the 4 LVDS transceivers are located very close together and are on both sides of the board, not all decoupling caps will be necessary. Please place as many as possible. Use fat traces to decoupling caps.
DECOUPLING REQUIREMENTS:

SINCE THE 4 LVDS TRANSCEIVERS ARE LOCATED VERY CLOSE TOGETHER AND ARE ON BOTH SIDES OF THE BOARD, NOT ALL DECOUPLING CAPS WILL BE NECESSARY. PLEASE PLACE AS MANY AS POSSIBLE. USE FAT TRACES TO DECOUPLING CAPS.
NOTE:
PLX VCC3_CTRL DECOUPLING IS ON A SEPARATE PAGE

PLX PCI9054 'J' Mode

ALE pull-down required in J-mode, all other unused address pins have internal pull-ups (see p12-1 PLX data book).

PLX-9054 MODE SELECTION
MODE[1:0] = '01' = J

100k GND# pull-up, as per PCI Spec.
100k RST# pull-up for benchtop debug.

(see PCI9054RDK-LITE for pull-up/down recommendations)
Cypress recommends a pull-down on TCK (p13 'Designing with Cypress ISR CPLDs for PC Cable Programming'). Internal pull-ups exist on TMS and TDI in accordance with the IEEE 1149.1 JTAG specification (p13 'Designing with Cypress ISR CPLDs for PC Cable Programming', and p2 'An Introduction to In-System Reprogramming with the Ultra37000'). TDO ... a pull-up/down. (A pull-up on TCK would also be acceptable. This resistance is to stop the clock pin from floating).
CHASSIS GROUND (ALONG THE EDGES OF THE CARDS AND THE CONNECTOR SHIELDS) IS TIED TO LOGIC GROUND (GND) AS OFTEN AS POSSIBLE ALONG THE PERIPHERAL OF THE BOARD.

PLACE AS MANY AS POSSIBLE USED 820pF, 500V, NPO DIELECTRIC CAPACITORS.

DEBUG POWER CONNECTIONS:

PLACE ON THE UNDERSIDE OF THE PCB, BY THE CPCI CONNECTOR NEAR THE APPROPRIATE POWER PLANE. THESE PADS WILL BE USED TO CONNECT TEMPORARY POWER SUPPLIES DURING INITIAL DEBUG.

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Risetime Control Schmitt Triggers

CF_MRDY# AND CF_CORL_DONE ARE PULLED LOW OR TRI-STATED BY THE CORRELATOR FPGA. PULL-UPS FOR THESE SIGNALS ARE REQUIRED AT THE SYSTEM CONTROLLER. PULL-UPS ARE REQUIRED ON CF_PS_DONE AND CF_PS_STATUS# DUE TO THEIR TRISTATING NATURE, AND A PULL-UP IS REQUIRED ON CF_PS_CONFIG# (THE PULL-UP IS ON THE BUFFERS PAGE).

The (green) DONE LED lights when the FPGAs are successfully configured.

The (red) STATUS LED lights when there is an FPGA configuration error.

NOTE: THIS IS A (FAIRCHILD OR MOTOROLA) 5V PART, AS A FUNCTIONALLY EQUIVALENT 3.3V PART WAS NOT AVAILABLE.

NOTE: THIS IS A 1-of-10 FPGA RAM READ/WRITES (THE APPROPRIATE SEL# SIGNAL IS ASSERTED FOR EVERY WORD OF DATA TRANSFERRED FROM THE FPGA RAM). OTHERWISE OUTPUTS ARE HIGH TO ENSURE THIS. ENSURE THAT CF_SEL[8..0] = HIGH WHEN FPGA RAM IS NOT BEING ACCESSED.

1-of-10 Correlator FPGA Select
The two DS18B20 devices are powered differently so that their physical location can be identified. One device is placed under FPGA1, the other under FPGA7.
REVISION HISTORY

Schematic revision A.3 to B.0 changes

<table>
<thead>
<tr>
<th>Page</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>p3</td>
<td>Changed XF[1..0] to DSP_XF[1..0]. Added DSP_MA18 to the DSP RAM block. Added the following clock ports: CLK_SYS_CON, CLK_SDR[1..0], CLK_MICTOR[2..0] Deleted CLK_GPB[1..0] Renamed CLK_33MHz_PCI to CLK_33MHz_FANOUT</td>
</tr>
<tr>
<td>p10</td>
<td>Renamed CLK_33MHz_PCI to CLK_33MHz_FANOUT Added pull-down to TCLK_REF (R654)</td>
</tr>
<tr>
<td>p13</td>
<td>Renamed CLK_33MHz_PCI to CLK_33MHz_FANOUT. Added a pull-down to CLK_33MHz_FANOUT (R695).</td>
</tr>
<tr>
<td>p22, p25, p28, p34, p37, p43, p46, p49</td>
<td>Added 0-Ohm jumper in TDI path (R692, R681, R690, R659, R664, R663, R655, R658, R667, R656). Added a test point to TDI (TP844, TP843, TP842, TP841, TP846, TP845, TP837, TP840, TP839, TP838)</td>
</tr>
<tr>
<td>p55</td>
<td>Changed XF[1..0] to DSP_XF[1..0]. Added a pull-up stuff option to DSP_RST# (R665). Added pull-downs to DSP_TCLK[1..0] since they reset to inputs (R693, R694)</td>
</tr>
<tr>
<td>p56</td>
<td>Fixed the part description for the Flash RAM and added DSP_MA18 pin and net. Added DSP_MA18 to the hierarchy address port.</td>
</tr>
<tr>
<td>p56</td>
<td>Deleted the 2-pin headers. Added pull-ups to TDI (R657). Added 0-ohm jumpers in TDI path (R668, R669). Added pull-downs to EPROM data outputs (R670, R671).</td>
</tr>
<tr>
<td>p68</td>
<td>Deleted CLK_GPB[1..0] port. Added CLK_SYS_CON, CLK_SDR[1..0], CLK_MICTOR[2..0] ports. Fixed Mictor header to HP5346A pinout.</td>
</tr>
<tr>
<td>p69</td>
<td>Rearranged the page layout. Changed the nets: CF_MRDY_STO# to CF_MRDY_STO CF_PS_STATUS_STO# to CF_PS_STATUS_STO CF_PS_DONE_STO to CF_PS_DONE_STO CF_CORI_DONE to CF_CORI_DONE_STO# to reflect the inverting nature of the Schmitt triggers. Changed the pin names on the FPGA part. Deleted R412 (CONFIG pull-down). Added pull-ups to MSELB, MSELG, MSELJ, MSELK (R652, R693, R654, R655). Added a current-limiting resistor in TDO path (R686). Renamed pin AF20 from TPO to TP1. Renamed pin PS from CLK_SDR to TP2. Added pull-down to TP2 (R687). Added test points to TP1 and TP2 (TP857, TP858). Added 20 test points to CF control signals (TP859, TP860, TP861, TP862, TP863, TP864, TP865, TP866, TP867, TP868, TP869, TP870, TP871, TP872, TP873, TP874, TP875, TP876, TP877, TP878).</td>
</tr>
<tr>
<td>p70</td>
<td>Placed a no mount box around R161 (PCI_RST# pull-up). Enabled the NAND-gates U29C, U29D, U29E (using a single pull-up R690). Enabled the one-shot U63B, using a pull-down (R689) and a pull-up (R688). Added 9 test points to the DSP control signals (TP895, TP890, TP881, TP882, TP883, TP884, TP885, TP886, TP887).</td>
</tr>
<tr>
<td>p71</td>
<td>Removed pin P5 = SDR_CLK. Deleted CLK_GPB[1..0]. Added CLK_SYS_CON, CLK_MICTOR[1..0], CLK_SDR[1..0]. Routed the new clocks. Fixed up the Mictor headers. Replaced R99 with R691 and R692. Added test points to the SDRAM controls (TP888, TP889, TP890, TP891, TP892, TP893, TP894, TP895, TP896, TP897). Updated the SDRAM to the Hyundai part.</td>
</tr>
</tbody>
</table>
### Revision History

**Schematic revision B.0 to B.1 changes**

<table>
<thead>
<tr>
<th>Page</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>p2</td>
<td>Added a 'Serial ID and board configuration EEPROM' box.</td>
</tr>
<tr>
<td>p3</td>
<td>Removed: JTAG_TCKA, JTAG_TCKB, JTAG_TMSA, JTAG_TMSB, PCI_CBE[3..0], PCI_INTB, PCI_INTCA, PCI_INTD#</td>
</tr>
<tr>
<td></td>
<td>Added: JTAG_TCK[3..0], JTAG_TMS[3..0], CF_CORL_MODE[1..0], CF_CORL_MODE_IN[1..0], CF_CORL_MODE_OUT[1..0], SYS_LED[1..0], SYS_RST#, CLK_DSP_XTAL, CF_MWR, CF_BUF_OE#</td>
</tr>
<tr>
<td></td>
<td>p22, 25, 28, 31, 34, 37, 40, 43, 46, 49</td>
</tr>
<tr>
<td></td>
<td>Changed TP1 and TP2 to CORL_MODE1 and MWR, Changed TDI resistors (R662, R661, R660, R659, R684, R663, R655, R658, R587, R586) to 100E.</td>
</tr>
<tr>
<td></td>
<td>Added CE# 100E resistors: R591, R705, R706, R707, R708, R709, R710, R711, R712, R713.</td>
</tr>
<tr>
<td></td>
<td>Added SMT LEDs: D8, D9, D10, D11, D12, D13, D14, D15, D16, D17.</td>
</tr>
<tr>
<td></td>
<td>p55</td>
</tr>
<tr>
<td></td>
<td>Changed the INTA# pull-down from 10K to 330E (required the addition of R731). Dual source terminated the DSP XTAL so that the clock could be routed to the system controller (added R730).</td>
</tr>
<tr>
<td>p9</td>
<td>U80 faced extensive rework: removed all JTAG related signals, fanned out the Passive Serial configuration signals, CF_MWR added, LED[3..0] added, and CF_CORL_MODE changed to CF_CORL_MODE0 and added CF_CORL_MODE1. Added CF_BUF_OE# to control the data buffer outputs. The LEDs in the quad-tower that were previously power-supply indicators are now controllable by the system controller.</td>
</tr>
<tr>
<td></td>
<td>Added resistors: R697, R698, R699, R700, R701, R702, R703, R704</td>
</tr>
<tr>
<td></td>
<td>Moved resistor: R500</td>
</tr>
<tr>
<td>p12</td>
<td>Changed R494, R495 to 10k, R496 to R497 to 330E.</td>
</tr>
<tr>
<td>p13</td>
<td>Changed R455, R464, R465, R457, R458, R459 to 10k, R460, R461, R462 to R464, R465, to 330E.</td>
</tr>
<tr>
<td>p16</td>
<td>Added CF_MWR, changed CF_CORL_MODE to CF_CORL_MODE0 and added CF_CORL_MODE1. Changed CF_PS_DCLK and DATA to CF_PS_DCLK[1..0] and CF_PS_DATA[1..0], changed CF_JTAG_TCKA to CF_JTAG_TCK[2..0], CF_JTAG_TMS[2..0].</td>
</tr>
<tr>
<td>p18,</td>
<td>Changed the TDI resistors R668, R669 to 100E. Added TDO resistor R732. Added DCLK pull-downs R733, R734.</td>
</tr>
<tr>
<td>p19</td>
<td>Implemented additional fanout of the JTAG TCK and TMS signals. Added dual buffers U89, U90, U91, U92. Added resistors R742, R743, R744, R745, R746, R747, R748, R749, R750, R751, R752, R753. Added C64, C65, C66, C67.</td>
</tr>
<tr>
<td>p59</td>
<td>Added SMT LEDs to Passive Serial STATUS and DONE (D18, D19, R735, R736). Added R765 in TDO.</td>
</tr>
<tr>
<td>p60, 61, 62, 63</td>
<td>Added R724, R725, R726, R727, R737, R738 to the unused channel on the LVDS connector.</td>
</tr>
<tr>
<td>p64</td>
<td>Replaced U88 OP491 with OP462. Replaced U69 OP191 with OP262. Used extra op-amp in the OP262 to buffer the output of the AD22100.</td>
</tr>
<tr>
<td>p65</td>
<td>Removed PCI_INTB#, C#, D#. Renamed GP_C/BE[3..0] as test points TP[3..0]. Added SYS_RST#. Added 100k-Ohm pull-up to PCI_GNT#. Added a 10kE resistor to PCB_JTAG_TDO (R766). Added test points to the PCI signals: TP903 to TP921.</td>
</tr>
<tr>
<td>p66</td>
<td>Moved the LEDs to the buffer page.</td>
</tr>
<tr>
<td>p67</td>
<td>Changed the following:</td>
</tr>
<tr>
<td></td>
<td>PIN: TP WAS NOW</td>
</tr>
<tr>
<td></td>
<td>AD5 TP873 CF_CORL_MODE CF_CORL_MODE0</td>
</tr>
<tr>
<td></td>
<td>P5 TP857 TP2 CF_CORL_MODE1</td>
</tr>
<tr>
<td></td>
<td>AF20 TP858 TP1 CF_CORL_DONE#</td>
</tr>
<tr>
<td></td>
<td>M22 TP726 GP_CBE#0 CF_MWR</td>
</tr>
<tr>
<td></td>
<td>L26 TP727 GP_CBE#1 CF_BUF_OE#</td>
</tr>
<tr>
<td></td>
<td>L25 TP728 GP_CBE#2 SYS_LED0</td>
</tr>
<tr>
<td></td>
<td>L24 TP729 GP_CBE#3 SYS_LED1</td>
</tr>
<tr>
<td></td>
<td>P3 TP895 DGM1 ONEWIRE_IN#</td>
</tr>
<tr>
<td></td>
<td>P1 TP896 DGM2 ONEWIRE_OUT</td>
</tr>
<tr>
<td></td>
<td>N5 TP897 DGM3 ONEWIRE_ENABLE</td>
</tr>
<tr>
<td></td>
<td>A14 TP675 CLK_DSP_XTAL CLK_DSP_H1</td>
</tr>
<tr>
<td></td>
<td>A13 TP871 CF_CORL_DONE# CLK_DSP_H1</td>
</tr>
<tr>
<td>p68</td>
<td>Added SMT LEDs to Passive Serial STATUS and DONE (D18, D19, R735, R736). Added R765 in TDO.</td>
</tr>
<tr>
<td>p69</td>
<td>Added SMT LEDs to Passive Serial STATUS and DONE (D18, D19, R735, R736). Added R765 in TDO.</td>
</tr>
<tr>
<td>p70</td>
<td>Added SYS_RST# a pull-up (R767) and used the spare NAND gates in U29 to hook it up. Added the 1-Wire bus buffers (U93, U94, R754, R755, R756, R757, C2902, C2993) and the 1-Wire EEPROM (U96) and temperature sensor (U95).</td>
</tr>
</tbody>
</table>
| p71  | Added R760, R761, R762, R763 to the GGG control signals. Added SDRAM signals to the Mictor header. Re-routed DQM to all 4 DQM ports (added R764). Added pull-up/down to DQM (R758, R759). Added pull-ups to the SDRAM data bus RP72 to RP79.
REVISION HISTORY

Schematic revision B.1 to B.2 changes

General: BOM updated, footprints updated. Netlist taked into PADs PowerPCB and components placed. Some net name errors were cleaned up during layout and routing. NO MOUNT component names were appended with -nm for clarity.

7/20/00: DWH reviewed the Rev. B.2. PCB layout and determined that the following components needed to be added:

<table>
<thead>
<tr>
<th>Page</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>p53</td>
<td>9 decoupling caps added to improve FPGA#9 decoupling to VCC_INT. CD904 to CD912.</td>
</tr>
<tr>
<td>p54</td>
<td>9 decoupling caps added to improve FPGA#9 decoupling to VCC_IO. CD913 to CD921.</td>
</tr>
<tr>
<td>p58</td>
<td>U89 and U91 VCC3_CTRL changed to VCC3_IO due to component placement.</td>
</tr>
<tr>
<td>p65</td>
<td>Added 6 TPs TP922 to TP927.</td>
</tr>
<tr>
<td>p70</td>
<td>Changed DS1820 VCC3_CTRL to VCC3_IO due to placement. Added 3 TPs TP928 to TP930.</td>
</tr>
</tbody>
</table>