GDA 9809 - DIGITIZER BASE BOARD FOR CALTECH

SEE THE HEIRARCHY MAP ON p4 FOR THE MAP OF PAGE NUMBERS TO HEIRARCHICAL BLOCKS.

Revision C.1

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Cover Page
The H? references in the folder shapes indicate the hierarchy block number(s) associated with the folder name. The p? references next to the folder shapes indicate the page number of the schematic in OrCAD 9.1.
There are three options for JTAG chains. The first option is used for board debugging and initial bring-up of the boards. Using the external header and by shorting pins 1 and 2 of the jumper block, a single device JTAG chain is formed with the system controller. In the second option, it is assumed that the system controller is tri-stated, or at least, is not driving JTAG_SEL low and that jumper pins 2 and 3 are shorted. This forms a 6 device JTAG chain.

In the third option, the multiplexer is used to control the digitizer FPGA and EPROM JTAG chain. The 4 digitizer FPGAs (0 to 3) are consecutively linked in the JTAG chain followed by the system controller EPROM.

When the system controller is configured, the system controller can drive JTAG_SEL low and then the JTAG signals for the digitizer FPGA chain will originate from the system controller. This option can be used for digitizer FPGA configuration instead of passive serial configuration and it can be used to reprogram the EPROM. The JTAG chain can also be used for boundary scan tests originating from the JTAG header or the PCI interface. A jam player located in the host computer or in the board DSP can be used for controlling this JTAG interface.

Resistor pads are available to short TDI and TDO on the 4 FPGAs. This allows a reduced number of FPGAs to be loaded while still completing the JTAG chain.
ROUTE +/-12 FROM THE PCI CONNECTOR TO THE MICTOR CONNECTOR USING FAT TRACES ON ANY APPROPRIATE SIGNAL OR POWER PLANE.

GROUND AND CHASSIS GROUND ARE TIED TOGETHER AS OFTEN AS POSSIBLE (EVERY INCH) WITH A CAPACITOR.

VCC_INT IS REQUIRED ONLY BY THE DIGITIZER FPGAS AND VTTL IS REQUIRED ONLY BY SOME OF THE CONTROL CIRCUITS AND THE DELAY CHIP. PLACES WHERE VTTL OR VCC_INT ARE NOT REQUIRED CAN BE USED TO DISTRIBUTE POWER TO THE DIGITIZER MODULE CONNECTORS.

VCC3 IS SEGMENTED FOR THE FPGA IO SUPPLIES, THE LVDS CHIPS, AND THE CONTROL LOGIC. THE PLACEMENT OF COMPONENTS SHOULD ACCOUNT FOR THE VCC3 BACKBONE. THIS BACKBONE MUST NOT BE COMPROMISED BY NUMEROUS VIAS.
AN EXAMPLE ROUTING FOR THE DIGITIZER BOARD. BUSES A AND B FROM THE
MODULE CARRY 32-BIT DATA FROM TWO DIGITIZERS LOCATED ON THE MODULE
TO THE FOUR DIGITIZER FPGAS. THE FPGAS PERFORM QUANTISATION PATTERN
COUNTING, DELAY LINE, AND AUTOCORRELATION FUNCTIONS AND TRANSMIT A
COPY OF THE DATA TO THE FOUR LVDS TRANSCEIVERS.
NOTE:
The bidirectional buffers for bits DSP_DQ[7:0] must be 5V tolerant to support reads from the 5V AD7828 ADC.

**DIAGRAM**

- DATA BUS BUFFERS
- ADDRESS BUS BUFFER
- CONTROL SIGNAL BUFFER
- PASSIVE SERIAL END TERMINATIONS

**ATTEMPT TO PLACE A DECOUPLING CAP ON EVERY VCC PIN**

- **LED0**, **LED1**, **LED2**, **LED3**

**DIAGRAMERY**

- **NOTE:**
  - DIR = 0 B -> A WRITE TO DIGITIZER FPGAS
  - DIR = 1 A -> B READ FROM DIGITIZER FPGAS
DSP ADDRESS AND DATA BUS PULL-UPS AND PULL-DOWNS

DIGITIZER FPGA ADDRESS AND DATA BUS PULL-UPS AND PULL-DOWNS

DECOUPLING CAPACITORS FOR THE VCC_CTRL RESISTOR PACKS.

DECOUPLING FOR THE VCC_IO RESISTOR PACKS.

USE VCC3_CTRL IF RESISTORS ARE PLACED NEAR TO BUFFERS. USE VCC3_IO IF RESISTORS ARE PLACED AT THE END OF THE BUS.
DECOUPLING CAPACITORS FOR THE SYSTEM CONTROLLER FPGA VCC_INT PINS.
EVERY VCC_INT PIN SHOULD HAVE A DECOUPLING CAPACITOR CLOSE BY.

DECOUPLING CAPACITORS FOR THE PLX-9054 PCI MASTER/TARGET.
EVERY VCC/GND PIN SHOULD HAVE A DECOUPLING CAPACITOR CLOSE BY.

DECOUPLING CAPACITORS FOR THE DSP.
EVERY VCC PIN SHOULD HAVE A DECOUPLING CAPACITOR CLOSE BY.
DECOUPLING PROCEDURE FOR THE DIGITIZER FPGAS:

SINCE THE 4 FPGAS ARE LOCATED SO CLOSE, MANY OF THE DECOUPLING CAPS PLACED WILL PERFORM DECOUPLING FOR MORE THAN 1 FPGA. PLACE AS MANY OF THESE DECOUPLING CAPACITORS AS POSSIBLE. THE DENSITY OF DECOUPLING SHOULD BE UNIFORM OVER THE VCC_INT SEGMENT AND SHOULD BE SIMILAR TO THE VCC3_IO DECOUPLING.
DECOUPLING PROCEDURE FOR THE DIGITIZER FPGAS:

SINCE THE 4 FPGAS ARE LOCATED SO CLOSE, MANY OF THE DECOUPLING CAPS PLACED WILL PERFORM DECOUPLING FOR MORE THAN 1 FPGA. PLACE AS MANY OF THESE DECOUPLING CAPACITORS AS POSSIBLE. THE DENSITY OF DECOUPLING SHOULD BE UNIFORM OVER THE VCC3_IO SEGMENT AND SHOULD BE SIMILAR TO THE VCC_INT DECOUPLING.
CONTROL SIGNALS

JTAG PROGRAMMING SIGNALS

PASSIVE SERIAL PROGRAMMING SIGNALS

PASSIVE SERIAL CONFIGURATION: SEE AN-69, FIGURE 8. PAGE 8. THE DIGITIZER FPGAS ARE CHAINED FPGA 0 TO FPGA 3.

JTAG CONFIGURATION: SEE AN-88, FIGURE 1, PAGE 2. THE DIGITIZER FPGAS ARE CHAINED FPGA 0 TO FPGA 3.

DIGITIZER FPGA CONTROL BLOCK 0

DIGITIZER FPGA CONTROL BLOCK 1

DIGITIZER FPGA CONTROL BLOCK 2

DIGITIZER FPGA CONTROL BLOCK 3
These two resistors allow the JTAG and Passive Serial chains to be preserved if an FPGA is not loaded.

1. These two resistors allow the JTAG and Passive Serial chains to be preserved if an FPGA is not loaded.
2. The resistors on DF_PS_CE# and DF_JTAG_TDO allow an FPGA that is loaded to be jumped over (use this to avoid a loaded, but dead FPGA).

A THIS SURFACE MOUNT LED LIGHTS WHEN THE FPGA IS CONFIGURED (PASSIVE SERIAL OR JTAG CONFIGURATION).

B LED_SMT

C THIS SURFACE MOUNT LED LIGHTS WHEN THE FPGA IS CONFIGURED (PASSIVE SERIAL OR JTAG CONFIGURATION).

D IF AN FPGA IS CONFIGURED (PASSIVE SERIAL OR JTAG CONFIGURATION).

E LED_SMT

F DF_ADDR[13..0]

G INTERFACE ADDRESS AND DATA BUS

H DF_R/W#

I DF_WAIT#

J DF_CORL_RST#

K DF_PS_CONFIG#

L DF_PS.Done

M DF_PS.STATUS#

N DF_PS_CE#

O (A 1K PULL UP IS RECOMMENDED ON EACH TDI IN THE JTAG CHAIN - ALTERA HOTLINE)

P DF_CORL_DONE#

Q DF_PS_CE#_TP

R DF_JTAG_TDI

S DF_JTAG_TDO

T DF_PS_CONFIG#_TP

U DF_PS.Done

V DF_PS.STATUS#_TP

W DF_PS_CE#_TP

X DF_PS_CE#_TP

Y DF_PS_CE#_TP

Z BGA TEST POINTS

SEE ALTERA AN-59 AND THE BYTEBLASTER DATA SHEET FOR MORE DETAILS ON PASSIVE SERIAL CONFIGURATION. DF_PS_CONFIG#, DF_PS_DONE, AND DF_PS_STATUS# (SIGNS COMMON TO THE 4 DIGITIZER FPGA) ARE PULLED UP WITH 1K BACK AT THE SYSTEM CONTROLLER. AN-59, FIGURE 8, PAGE 8 SHOWS THE PASSIVE SERIAL CHAIN IMPLEMENTED IN THIS SYSTEM.
DF_RDY# AND DF_CORL_DONE ARE PULLED LOW OR TRI-STATED BY THE DIGITIZER FPGA. PULL-UPS FOR THESE SIGNALS ARE LOCATED AT THE SYSTEM CONTROLLER.

INTERFACE ADDRESS AND DATA BUS

READ/WRITE CONTROL

CORRELATION CONTROL

PASSIVE SERIAL CONFIGURATION CONTROL

JTAG INTERFACE

CLOCK

TEST POINTS

1. These two resistors allow the JTAG and Passive Serial chains to be preserved if an FPGA is not loaded.

2. The resistors on DF_PS_CE# and DF_JTAG_TDO allow an FPGA that is loaded to be jumped over (use this to avoid a loaded, but dead FPGA).

SEE ALTERA AN-59 AND THE BYTEBLASTER DATA SHEET FOR MORE DETAILS ON PASSIVE SERIAL CONFIGURATION. DF_PS_CONFIGA, DF_PS_DONE, AND DF_PS_STATUS# (SIGNALS COMMON TO THE 4 DIGITIZER FPGAS) ARE PULLED UP WITH 1K BACK AT THE SYSTEM CONTROLLER. AN-59, FIGURE 8, PAGE 8 SHOWS THE PASSIVE SERIAL CHAIN IMPLEMENTED IN THIS SYSTEM.
DIGITIZER FPGA NUMBER: 2

JTAG / PASSIVE SERIAL STUFF OPTIONS:
1. These two resistors allow the JTAG and Passive Serial chains to be preserved if an FPGA is not loaded.
2. The resistors on DF_PS_CE# and DF_JTAG_TDO allow an FPGA that is loaded to be jumped over (use this to avoid a loaded, but dead FPGA).

DIGITIZER FPGA Part B-Control/Digitizer FPGA Part B-Control
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SEE ALTERA AN-59 AND THE BYTEBLASTER DATA SHEET FOR MORE DETAILS ON PASSIVE SERIAL CONFIGURATION. DF_PS_CONFIG, DF_PS_DONE, AND DF_PS_STATUS# (SIGNALS COMMON TO THE 4 DIGITIZER FPGAS) ARE PULLED UP WITH 1K BACK AT THE SYSTEM CONTROLLER. AN-59, FIGURE 8, PAGE 8 SHOWS THE PASSIVE SERIAL CHAIN IMPLEMENTED IN THIS SYSTEM.
This surface mount LED lights when the FPGA is configured (passive serial or JTAG configuration).

DF_ADDR[13..0] are pulled low or tri-stated by the digitizer FPGA. Pull-ups for these signals are located at the system controller.

DF_PS_CONFIG#, DF_PS_DONE, AND DF_PS_STATUS# (SIGNS COMMON TO THE 4 DIGITIZER FPGAS) ARE PULLED UP WITH 1K BACK AT THE SYSTEM CONTROLLER. AN-59, FIGURE 8, PAGE 8 SHOWS THE PASSIVE SERIAL CHAIN IMPLEMENTED IN THIS SYSTEM.
Supplementary decoupling is shown on the power distribution page.
Current Requirement Estimates:

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Estimate</th>
</tr>
</thead>
<tbody>
<tr>
<td>VECL</td>
<td>7.3A</td>
</tr>
<tr>
<td>VTT</td>
<td>9.0A</td>
</tr>
<tr>
<td>VCC</td>
<td>1.4A</td>
</tr>
<tr>
<td>VCC3</td>
<td>0.5A</td>
</tr>
<tr>
<td>+12V</td>
<td>0.2A</td>
</tr>
</tbody>
</table>

Assuming the bus connections (P1-P15) can handle 1A per pin, then assigning a block of 5 on each connector for VECL and VTT should be adequate. Assuming the regular pins can handle 100mA, then VCC requires 14 pins, VCC3 requires 5, and +12V requires 2. The connector pinout reflects this analysis.
CLK_DM_B[3..0] are nominally 62.5MHz. They are routed to FPGAs 0 to 3.

CLK_LVDS_TX[3..0] frequency is selected by a MUX on the Digitizer Module. These clocks are routed to LVDS Transceiver Blocks 0 to 3.
PLACE ALL RESISTORS NEAR THE LOAD (RAM END)

PULL-UP/DOWNS FOR SIGNAL QUALITY TUNING.
10K PULL-UPS ARE NECESSARY TO DEASSERT CONTROL SIGNALS WHEN NO DRIVING SIGNAL IS PRESENT.

DO NOT STUFF PULL-DOWNS

10K PULL-UPS ARE NECESSARY TO DEASSERT CONTROL SIGNALS WHEN NO DRIVING SIGNAL IS PRESENT.
SYSTEM CONTROLLER CONFIGURATION EPROM

The power-on LOW-to-HIGH transition at the system controller CONFIG# pin initiates EPROM configuration. The SYS-FPGA drives CONF_DONE LOW and this drives CS# on the EPROM LOW. The FPGA then tri-states STATUS#, and since STATUS# is connected to OE, the pull-up resistor on OE enables the EPROMs. The EPC2 uses its internal oscillators to clock data to the system controller. When configuration is complete, CONF_DONE is tri-stated by the FPGA and the pull-up resistors on CS# disables the EPC2. See Altera AN-59 and the EPC data sheet for more details.

The configuration EPROM is located at the end of the JTAG chain. The system controller is first, then the 4 digitizer FPGAs, then the EPROM. The EPROM can be accessed over the JTAG chain via an external JTAG header, or via JTAG commands from the system controller. The system controller can be used to re-program the EPROM (and hence itself). Once reprogrammed, the system controller can issue a nINIT_CONF JTAG command and the system controller EPROM will reprogram the system controller.

The correlator FPGAs are configured using a passive serial interface from the system controller or via the JTAG chain.

LOCAL CLOCK GENERATION/FANOUT

The local bus clock operates asynchronously to the PCI clock. The DSP supports a clock frequency of up to 80MHz (5V version). The clock buffer shown here is pin-compatible with higher frequency parts.

Configuration EPROMs for FLEX Devices
Data Sheet: VCCSEL = VCC for 3.3V operation. VPPSEL = GND for 5V programming voltages, i.e., VPP = 5V (faster). Pull-up resistors are as per Fig. 4 of the data sheet.
This multiplexer is used to control the digitizer FPGA and EPROM JTAG chain. The 4 digitizer FPGAs (0 to 3) are consecutively linked in a JTAG chain followed by the system controller EPROM. On power-up, the system controller is tri-stated, so the pull-up resistor on JTAG_SEL selects signals originating in the header JTAG chain. Later, when the system controller is configured, the system controller can drive JTAG_SEL low and then the JTAG signals for the digitizer FPGA chain will originate from the system controller. This option can be used for digitizer FPGA configuration instead of passive serial configuration and it can be used to reprogram the EPROMs. The JTAG chain can also be used for boundary scan tests originating from the JTAG header or the PCI interface. A JAM player located in the host computer or in the board DSP can be used in controlling this JTAG interface.

The first FPGA in the Altera JTAG chain is the system controller. The signal SC_JTAG_TDO is the TDO output of the system controller FPGA. If PIN1 and PIN2 on this three pin header are shorted, then a 1 device JTAG chain is formed with only the system controller. If PIN2 and PIN3 are shorted, and JTAG_SEL = HIGH (the power-up default), then a 6 device JTAG chain is formed with the system controller, 4 digitizer FPGAs, and configuration EPROM.
DECOUPLING REQUIREMENTS:

SINCE THE 4 LVDS TRANSCEIVERS ARE LOCATED VERY CLOSE TOGETHER AND ARE ON BOTH SIDES OF THE BOARD, NOT ALL DECOUPLING CAPS WILL BE NECESSARY. PLEASE PLACE AS MANY AS POSSIBLE. USE FAT TRACES TO DECOUPLING CAPS.
SINCE THE 4 LVDS TRANSCEIVERS ARE LOCATED VERY CLOSE TOGETHER AND ARE ON BOTH SIDES OF THE BOARD, NOT ALL DECOUPLING CAPS WILL BE NECESSARY. PLEASE PLACE AS MANY AS POSSIBLE. USE FAT TRACES TO DECOUPLING CAPS.

TRANSMIT CLOCK IS NOT PRESENT IF MODULE IS DISCONNECTED.

THIS PART IS PLACED ON THE TOP SIDE OF THE PCB

THIS PART IS PLACED ON THE BOTTOM SIDE OF THE PCB

GND CHASSIS
LVDS TRANSCEIVER BLOCK:

DECOUPLING REQUIREMENTS:
SINCE THE 4 LVDS TRANSEIVERS ARE LOCATED VERY CLOSE TOGETHER AND ARE ON BOTH SIDES OF THE BOARD, NOT ALL DECOUPLING CAPS WILL BE NECESSARY. PLEASE PLACE AS MANY AS POSSIBLE. USE FAT TRACES TO DECOUPLING CAPS.

THIS PART IS PLACED ON THE TOP SIDE OF THE PCB

THIS PART IS PLACED ON THE BOTTOM SIDE OF THE PCB

THIS PART IS PLACED ON THE TOP SIDE OF THE PCB

TRANSMIT CLOCK IS NOT PRESENT IF MODULE IS DISCONNECTED

9809.dsn/LVDS Transceivers and Connector/LVDS Transceivers and Connector

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AD7828 requires 16mA of supply current. Ref-02 can supply 20mA, voltage references, such as AD696 and LT027, can only supply 10 to 15mA. If these devices are used and VTTL is within 0.3V of 5V, then the AD7828 can be connected to VTTL.

DAC-to-temperature conversion:

\[ T = \left( \frac{[\text{DAC reading}]/256 \times 5 + 97.5 \times 10^{-3}}{55.35 \times 10^{-3}} \right) \]

eg. \( T = 10 \) deg-C, \( V_{\text{IN}} = 1.6V \), \( V_{\text{OUT}} = 0.46V \), DAC = 17h

\[ V_{\text{OUT}} = 2.46 \times V_{\text{IN}} - 3.48V = T \times 55.35 \times 10^{-3} - 97.5 \times 10^{-3}V \]

For op-amp circuit design information see:

"Op-Amps for everyone", Ron Mancini, Texas Instruments, SLOD006A, Sept. 2001 (www.ti.com). Ch 4. was used to develop the AD22100 circuit.

Analog Devices, "Sensor Signal Conditioning", Ch 10 contains details on op-amp input protection.
NOTE: PLX VCC3_CTRL DECOUPLING IS ON A SEPARATE PAGE

PLX PCI9054 'J' Mode

ALE pull-down required in J-mode, all other unused address pins have internal pull-ups (see p12-1 PLX data book).

100k GNT# pull-up, as per PCI Spec.

100k RST# pull-up for benchtop debug.
Cypress recommends a pull-down on TCK (p13 'Designing with Cypress ISR CPLDs for PC Cable Programming'). Internal pull-ups exist on TMS and TDI in accordance with the IEEE 1149.1 JTAG specification (p13 'Designing with Cypress ISR CPLDs for PC Cable Programming', and p2 'An Introduction to In-System Reprogramming with the Ultra37000'). TDO...a pull-up/down. (A pull-up on TCK would also be acceptable. This resistance is to stop the clock pin from floating).

FOUR CLOCKS FROM LVDS (AVAILABLE ONLY WHEN THE DIGITIZER CARD HAS INPUT SIGNALS)

FOUR CLOCKS FROM DIGITIZER MODULE (ONLY CLOCKS 0 AND 3 AVAILABLE IN THE INITIAL COBRA SYSTEM)

THE CLOCKS FROM THE DIGITIZER MODULE CAN BE CHANGED USING THE ECL MULTIPLEXER ON THE MODULE (SEE THE DIGITIZER MODULE SCHEMATICS).

Ground points for the phase detector test points

Cypress recommends a pull-down on TCK (p13 'Designing with Cypress ISR CPLDs for PC Cable Programming'). Internal pull-ups exist on TMS and TDI in accordance with the IEEE 1149.1 JTAG specification (p13 'Designing with Cypress ISR CPLDs for PC Cable Programming', and p2 'An Introduction to In-System Reprogramming with the Ultra37000'). TDO is an output, so does not require a pull-up/down. (A pull-up on TCK would also be acceptable. This resistance is to stop the clock pin from floating).
CHASSIS GROUND (ALONG THE EDGES OF THE CARDS AND THE CONNECTOR SHIELDS) IS TIED TO LOGIC GROUND (GND) AS OFTEN AS POSSIBLE ALONG THE PERIPHERAL OF THE BOARD.

PLACE AS MANY AS POSSIBLE VCC3 FOR FPGA IOs

BULK DECOUPLING FOR VCC3

VCC3 FOR FPGA IOs

VCC3 FOR THE CONTROL LOGIC

VCC3 FOR THE LVDS TRANSCEIVERS

CLEAN TTL SUPPLY FOR THE DELAY CHIP, JTAG INTERFACE, PHASE DETECTOR, EPC2, AD7828.

SYSTEM CONTROLLER FPGA CORE SUPPLY

(2.5V OR 3.3V)

FLEX10K100E 2.5V CORE SUPPLY

BULK DECOUPLING FOR +12V

(ROUTED TO MODULE CONNECTOR)

NOTE: DO NOT MOUNT.

THIS OPTION IS FOR 5VDSP CHIP AT HIGHER SPEEDS.

Do not mount these caps. These points will be used for power supply connections. Place on the underside of the PCB, near the cPCI connectors, close to their respective power planes.

FLEX10K100A 3.3V CORE SUPPLY

BULK DECOUPLING FOR FPGA

VCC_INT (3.3V OR 2.5V)

VCC3_CTRL

VCC3_LVDS

VECL

VTT

NOTE: OUTPUT CAP MUST HAVE
ESR = 50-mOhm to 1.5-Ohm

DSP POWER SUPPLY

(3.3V OR 5V)

DSP_PWR

BULK DECOUPLING FOR THE MODULE ECL SUPPLIES

VECL AND VTT ARE ONLY USED ON THE DIGITIZER MODULE. THE DECOUPLING CAPACITORS ACT AS CHARGE RESERVOIRS FOR THE MODULE POWER PLANES.
THESE SCHMITT TRIGGERS AVOID SLOW RISETIMES (DUE TO OPEN-DRAIN SIGNALS) AT THE FPGA.

DIGITIZER FPGA CONTROL

DIGITIZER FPGA PASSIVE SERIAL AND JTAG CONFIGURATION CONTROL

TEMPERATURE/VOLTAGE MONITOR AND PHASE DETECTOR ADC INTERFACE

SYSTEM CONTROLLER PASSIVE SERIAL/FRON INTERFACE

CONF_DONE

USER BUS

DIGITIZER FPGA CONFIGURATION STATUS LEDS

The (green) DONE LED lights when the FPGAs are successfully configured.

The (red) STATUS LED lights when there is an FPGA configuration error.

CF_MRDY# AND CF_CORL_DONE ARE PULLED LOW OR TRI-STATE BY THE CORRELATOR FPGA. PULL-UPS FOR THESE SIGNALS ARE REQUIRED AT THE SYSTEM CONTROLLER. PULL-UPS ARE REQUIRED ON CF_PS_DONE AND CF_PS_STATUS DUE TO THEIR TRISTATING NATURE. A PULL-DOWN IS REQUIRED ON CF_PS_CONFIG TO AVOID PUTTING THE CORRELATOR FPGAs IN PS MODE DURING POWER-UP.
STUFFING OPTION TO SELECT EITHER REF CLOCK FROM THE USER CONNECTOR OR LOCAL OSCILLATOR OR EXTERNAL SOURCE (SMB) (DEFAULT: FROM USER BUS CONNECTOR)

ALL CPU BACKPLANE CONNECTOR SHIELDS ARE TIED TO GROUND (POWER SUPPLY COMMON) NOT CHASSIS GROUND.

USER BUS WIDTH IS LIMITED TO 26-BITS DUE TO SYSTEM CONTROLLER PIN LIMITATIONS