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1 Introduction

This document describes the testing of the digitizer evaluation board which was used to prototype the digitizer circuits, and the correlator clock fanout circuits used in the COBRA correlator system.

The purpose of the initial testing of the digitizer evaluation board, performed during April to July 1999, was to confirm the operation of the correlator clock circuits so that the correlator boards could be completed and fabricated. Initial tests on the digitizer TDM circuits were performed to confirm basic operation, however, more complete analysis was left until the correlator prototypes were available. Poor performance of the PLLs during initial testing led to several weeks of PLL theoretical analysis and testing. This theory and analysis is documented in [13].

The first correlator boards (rev A.3) were fabricated and delivered in August 1999. Debugging and development of the system controller Verilog, DSP and PC control software, and correlator and digitizer FPGA VHDL, took most of the next year (a significant portion of time was spent debugging errors in the GDA-provided system controller and PCI cores). The correlator schematic and PCB were updated in July 2000 to include fixes and additional logic (rev B.2). Initial prototypes of the rev B.2 boards were delivered in Dec 2000.

Testing of the digitizer evaluation board was re-started in Nov 2000. This document summarizes the results of the 1999 and 2000 testing. The engineering specification in [12] contains a detailed description of the board design.

Two digitizer evaluation boards were loaded for testing; one board was fully loaded with both the correlator and digitizer logic, the other was loaded with only the digitizer logic. This document refers to the fully loaded board as #1 and the partially loaded board as #2.
2 Problems

This section contains a summary of issues/problems with the digitizer evaluation board. The solution to each problem, where relevant, is discussed in more depth elsewhere in this document. The issues/problems are listed in order of the component appearance in the schematic [11]:

- p9: the buffered 16MHz references (74F244 outputs) show ringing due to transmission line effects. The buffer outputs should have been source terminated.

- p9/p10/p11/p22/p23: the diodes loaded on the boards for the 3.3V clamps are in the wrong package. Confirm the correct part number/package type is used on the correlator and digitizer boards.

- p10/p13: the SY89421V PLLs required a 0.3V clamp (Schottky barrier diode) on the VCO control pin to stop the VCO control voltage exceeding the nominal bias voltage by more than 0.3V. Without this clamp, the VCO would become stuck and unlocked at 1.3GHz. The clamp caused an increase in reference spur levels. These spur levels were reduced by the use a 2nd order loop filter (resulting in a 3rd order PLL).

- p10/p13: the PLL control signals require pull-ups/downs to ensure valid controls during power-up prior to the system controller FPGA configuration.

- p11: the MPC949 control signals should have pull-ups/downs to ensure valid controls during power-up.

- p13: the -5V translation circuit for the TTL controls on the ECL-configured SY89421V PECL device did not work. Protection diodes on the BusSwitch prevented negative voltages being generated. A rework using a dual-supply analog switch fixed the problem.

- p13: high input leakage currents on the SY89421V TTL controls induced a large voltage drop over the 10kΩ pull-downs to -5V. These resistors needed to be reduced to 500Ω.

- p14: the 1GHz pulse masking circuit fails about 2% of the time. Timing analysis (ignoring PLL jitter) indicated that there should be available timing margin. The system controller does not seem to be at fault. Scope captures will have to be used to determine if the disable pulse is being generated during the time the circuit fails.

- p15: the threshold and reference buffer amplifier configurations required re-analysis. Higher-current drive op-amps are required to support the threshold voltage calibration routine.

- p15/p16: the decoupling capacitors on the reference voltages should have been placed close to the SPT7610 pins, on the same side of the PCB as the SPT7610 device.

- p15: replace through-hole components with surface mount.

- p16: the SPT7610 datasheet timing for DRA and DRB clocks are inverted with respect to the observed timing. This causes a potential setup/hold violation at the 100E445s that is corrected by a rework that swaps the 100EL14 clock buffer inputs.

- p16: the SPT7610 device on board#1 showed an incorrect output test pattern. The resulting test pattern made it appear that the TDM reset circuits were not operating correctly.

- p16: the input to the RF amplifier should be ac-coupled, and the final digitizer boards should allow for an input -3dB pad.

- p16: a 45kΩ was loaded instead of a 45Ω resistor on the RF amplifier output padding network.
• p16: dc-linearity testing requires that the RF input be removed. To allow for this option on the final digitizer boards, the input to the digitizer needs to be disabled either at the downconverter, or on the digitizer board with an RF switch or by removing power from the RF amplifier. These options need to be investigated.

• p17: inputs to the 100EL14 clock buffers need to be inverted to correct for the observed SPT7610 DRA/DRB timing.

• p20: the 100ELT25 ECL-to-TTL translators (single-source terminated and dual-source terminated) cannot drive at 128MHz.

• p23: A net assignment error on the LVDS transceiver input connections interchanged LT-DATA10 and LTDATA11 with respect to the output bus numbering. This can easily be corrected when mapping the data from digitizer output format to correlator format.

• p23: the decal numbering for the LVDS transceivers on the underside of the board are wrong, i.e., they are incorrectly numbered in a clockwise direction and pin 1 is in the wrong place. The chips were loaded correctly, so this is likely a silk error.

• p23: bus bits 10 and 11 flipped at the inputs to LVDS transceiver U27.

• p23: board #1 had a bad LVDS transceiver for bus bit 0 (U23).

• p24: the LVDS connector trace for LDCLK1 needs to be cut before interfacing with the correlator boards. This signal is grounded on the correlator boards.

• p26: Supply current requirement estimates show that the ferrite beads for VCC3_MPC, VTTL2, and VTTL3 were overrated (3A beads were used where 500mA beads would have sufficed). More critically, the ferrite bead for the SPT7610 digitizer power segment was underrated, a 500mA bead was used, whereas, the device requires 770mA. A 3A bead should have been used (two choices of beads were used on the board).

• p27: net naming errors on the system controller caused two shorts; EN_PULSE_MASK# with EN_DIGITIZER_CLK#, and THRESHOLD_CS# with THRESHOLD_R/W#. Reworks were required to fix these errors.

• p27: the Altera 10K30 (5V device) does not come in a TQFP-144 package. One digitizer evaluation board was loaded with a 10K30A (3.3V device) and the power pins were bussed together and routed to a 3.3V supply connection. The second board was loaded with a 10K20 device.

• p27: the data bus should have pull-up/down resistors to hold the bus at a valid logic level when no access is being performed. The address bus pull-ups/downs are optional, as this bus is always driven once the system controller FPGA is configured.

• p27: the Altera 10K20 requires a configuration EPROM. The system controller code for the digitizer module should be placed-and-routed in a MAX device or in a Cypress CPLD. These devices are EPROM based.

• p28: the digitizer control signal bus dig[d[2:0]] has bits 0 and 2 swapped on the converter output. This is corrected by swapping the pin assignments to bits 0 and 2 in the FPGA .acf file.

• p30: the op-amp U12 is powered from VCC directly. This connection should be to one of the VTTL planes. VCC is the power backbone and should only have ferrite beads on it (connecting to the power segments).
• p30: two of the op-amps (B and C) in the OP491 quad op-amp used for buffering the ADC0808 inputs have their input pads defined incorrectly. The schematic shows the pins correctly, however, connections on the board are wrong. Rework wires were required.

• p30: the unused op-amp in the OP491 quad op-amp package should have been disabled (recommended practice).

• p30: Analog Devices does not recommend that we use the REF-02 temperature output. We should use the AD22100 instead.

• p30: the ADC0808 does not have TTL compatible inputs. The minimum input high voltage for the control signals is VCC-1.5V = 3.5V (this was not observed to be a problem on the board loaded with the 3.3V FPGA, however, it could be if overlooked in a future design). The control inputs all need pull-ups to VCC.

• On the final PCB there were lots of unconnected capacitors surrounding the system controller FPGA that do not appear in the schematic. Clearly the PCB netlist was not properly compared to the schematic netlist before the boards were fabricated.

• The final digitizer modules need more via test pads, along with ground vias nearby. Probing the SPT7610 is especially hard. Via test points would make holding the oscilloscope probe and ground lead in place easier.
3 Initialization and power consumption

Prior to performing functionality tests of the digitizer evaluation boards, the power supply voltages, currents and noise, and power segment voltages, segment filter voltage drops, and segment noise require measurement. The supply currents were measured using a current probe. The supply and segment voltages were measured using an oscilloscope probe (with the exception of the 12V supply, which was measured using a voltmeter, as 12V exceeds the 'scope probe voltage range).

The digitizer evaluation board engineering specification contains estimates of the current required from each power supply, the recommended ferrite bead current rating, and shows that the voltage drop over the ferrite beads should be less than 50mV. Calculations in the engineering specification show that the ferrite bead for the digitizer power segment is underrated. The purpose of the tests in this section was to determine which other segments require higher rating beads.

ECL logic consumes the same amount of current regardless of operating frequency. Single-ended CMOS/TTL logic consumes current in proportion to the operating frequency. Differential LVDS drivers (CMOS) are current mode drivers, so their current consumption is approximately frequency independent. To obtain reasonable estimates of power consumption, the digitizer evaluation board should be connected to an RF source, and the digitizer should be digitizing the input (it should not be in test mode). The following initialization steps should be performed:

- Enable the TDM logic and select divide-by-8 mode (128MHz).
- Select one of the 128MHz output clocks.
- Enable the LVDS drivers.
- Pulse the threshold DAC reset line to ensure the thresholds are all reset to 800h (-0.5V), then set the plus and minus threshold voltages and load them. For example, set the plus threshold to 400h (-0.25V), and the minus threshold to C00h (-0.75V).

Other system controller default parameters are appropriate for the power supply tests. If the plus and minus threshold voltages are not changed, their reset state is 800h. The op-amps driving the ladder voltages are then trying to force the three ladder voltages to -0.5V. The OP491 op-amps are not able to sink the current required to hold these voltages at a common point and a 340kHz, 200mVpp oscillation is observed on the DAC -5V segment. The absolute source of this oscillation is not clear, however, setting the thresholds removes the oscillation (the plus threshold seems to dominate). Testing of higher current sourcing/sinking op-amps may help explain the cause of this observation.

Tables 1 and 2 show the supply measurements for the fully loaded digitizer evaluation board (board#1) and the partially loaded (board#2). The fully loaded board contains a 10K30A 3.3V FPGA for the system controller. The system controller 3.3V power is drawn from the VCC3_MPC segment.

Tables 1 and 2 show the actual voltages measured at, or close to, the supply connectors. The -5V and -2V supplies are generated using a lab supply, so it is possible to tune them close to -5V and -2V. The 5V, 3.3V, and 12V supplies are generated using an ATX-supply. The RMS ripple for the +5V, -5V, 3.3V, and -2V supplies was measured using the oscilloscope probes, and the ripple on the 12V supply was measured using the RMS setting on a voltmeter. A portion of the noise measured on all but the 12V supply is due to probe pickup. The probe grounds were connected via 3 inch ground leads clipped to the nearest SMB connector.

Tables 1 and 2 confirm that the supply voltages are within tolerance and that the measured currents are less than the current requirement estimates in the engineering specification. The power consumption of the two boards, i.e., 24W and 21W, is about 75% of the engineering specification estimate of 32.8W.
### Table 1: Power supply measurements for board#1.

<table>
<thead>
<tr>
<th>Supply</th>
<th>Voltage (V)</th>
<th>Current (A)</th>
<th>Power (W)</th>
<th>Ripple (mV_RMS)</th>
<th>Measurement Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5</td>
<td>4.97</td>
<td>0.5</td>
<td>2.5</td>
<td>37</td>
<td>CB57</td>
</tr>
<tr>
<td>-5</td>
<td>-5.00</td>
<td>2.4</td>
<td>12.0</td>
<td>32</td>
<td>connector</td>
</tr>
<tr>
<td>-2</td>
<td>-2.00</td>
<td>2.3</td>
<td>4.6</td>
<td>26</td>
<td>connector</td>
</tr>
<tr>
<td>3.3</td>
<td>3.41</td>
<td>1.2</td>
<td>4.1</td>
<td>28</td>
<td>CB61</td>
</tr>
<tr>
<td>12</td>
<td>12.05</td>
<td>&lt;0.1</td>
<td>&lt;1</td>
<td>7</td>
<td>C72</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>~24W</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 2: Power supply measurements for board#2.

<table>
<thead>
<tr>
<th>Supply</th>
<th>Voltage (V)</th>
<th>Current (A)</th>
<th>Power (W)</th>
<th>Ripple (mV_RMS)</th>
<th>Measurement Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5</td>
<td>5.01</td>
<td>0.4</td>
<td>2.0</td>
<td>33</td>
<td>CB57</td>
</tr>
<tr>
<td>-5</td>
<td>-5.00</td>
<td>2.4</td>
<td>12.0</td>
<td>36</td>
<td>connector</td>
</tr>
<tr>
<td>-2</td>
<td>-2.00</td>
<td>2.3</td>
<td>4.6</td>
<td>34</td>
<td>connector</td>
</tr>
<tr>
<td>3.3</td>
<td>3.45</td>
<td>0.4</td>
<td>1.4</td>
<td>39</td>
<td>CB61</td>
</tr>
<tr>
<td>12</td>
<td>12.02</td>
<td>&lt;0.1</td>
<td>&lt;1</td>
<td>7</td>
<td>C72</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>~21W</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Tables 3 and 4 show the voltage drops measured over the power supply segment ferrite beads. The beads are loaded as per the schematic. As expected, the voltage drop over the digitizer segment ferrite bead is larger than desired. These tests also show that the voltage drop over the PLL segment filters for both the ECL configured and LVPECL PLLs is greater than the desired maximum of 50mV.

On board#1 three reworks were performed:

- The 500mA ferrite bead loaded in FB5 (VLVPECL) was interchanged with the 3A ferrite bead loaded in FB26 (VTTL3). The voltage drop over FB5 (VLVPECL) was reduced to 5mV, and the drop over FB26 (VTTL3) increased to 26mV.

- The 500mA ferrite bead loaded in FB21 (digitizer segment) was interchanged with the 3A ferrite bead loaded in FB19 (VTTL1). The voltage drop over FB21 (digitizer segment) was reduced to 6mV, and the drop over FB19 (VTTL1) increased to 78mV. The voltage drop over the VTTL1 ferrite bead now exceeds the 50mV requirement.

- The 500mA ferrite bead loaded in FB22 (ECL PLL segment) was interchanged with the 3A ferrite bead loaded in FB24 (VTTL2). The voltage drop over FB22 (ECL PLL segment) was reduced to 7mV, and the drop over FB24 (VTTL2) increased to 93mV. Again, the voltage drop over the VTTL2 ferrite bead now exceeds the 50mV requirement.
Table 3: Power segment voltage measurements for board#1.

<table>
<thead>
<tr>
<th>Supply/Segment</th>
<th>Ferrite Bead</th>
<th>V_{supply} (V)</th>
<th>V_{segment} (V)</th>
<th>∆V (mV)</th>
<th>Ripple (mV_{RMS})</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VTTL1</td>
<td>FB19</td>
<td>4.984</td>
<td>4.981</td>
<td>3</td>
<td>41</td>
</tr>
<tr>
<td>VTTL2</td>
<td>FB24</td>
<td>4.981</td>
<td>4.978</td>
<td>3</td>
<td>41</td>
</tr>
<tr>
<td>VTTL3</td>
<td>FB26</td>
<td>4.981</td>
<td>4.980</td>
<td>1</td>
<td>38</td>
</tr>
<tr>
<td>AAVCC+5</td>
<td>FB18</td>
<td>4.975</td>
<td>4.974</td>
<td>1</td>
<td>40</td>
</tr>
<tr>
<td>-5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PLL</td>
<td>FB22</td>
<td>-4.990</td>
<td>-4.880</td>
<td>110</td>
<td>31</td>
</tr>
<tr>
<td>TDM</td>
<td>FB20</td>
<td>-4.987</td>
<td>-4.973</td>
<td>14</td>
<td>34</td>
</tr>
<tr>
<td>FIL</td>
<td>FB17</td>
<td>-5.013</td>
<td>-4.973</td>
<td>40</td>
<td>36</td>
</tr>
<tr>
<td>SPT</td>
<td>FB21</td>
<td>-5.010</td>
<td>-4.796</td>
<td>214</td>
<td>33</td>
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<tr>
<td>DAC</td>
<td>FB16</td>
<td>-5.008</td>
<td>-5.000</td>
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<td>32</td>
</tr>
<tr>
<td>3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VLVPECL</td>
<td>FB5</td>
<td>3.409</td>
<td>3.210</td>
<td>199</td>
<td>29</td>
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<tr>
<td>VCC3_MPC</td>
<td>FB25</td>
<td>3.405</td>
<td>3.402</td>
<td>3</td>
<td>30</td>
</tr>
<tr>
<td>VCC3_LVDS</td>
<td>FB23</td>
<td>3.402</td>
<td>3.398</td>
<td>4</td>
<td>30</td>
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</table>

Table 4: Power segment voltage measurements for board#2.

<table>
<thead>
<tr>
<th>Supply/Segment</th>
<th>Ferrite Bead</th>
<th>V_{supply} (V)</th>
<th>V_{segment} (V)</th>
<th>∆V (mV)</th>
<th>Ripple (mV_{RMS})</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VTTL1</td>
<td>FB19</td>
<td>5.007</td>
<td>5.006</td>
<td>1</td>
<td>35</td>
</tr>
<tr>
<td>VTTL2</td>
<td>FB24</td>
<td>5.011</td>
<td>5.008</td>
<td>3</td>
<td>33</td>
</tr>
<tr>
<td>VTTL3</td>
<td>FB26</td>
<td>5.011</td>
<td>5.007</td>
<td>4</td>
<td>30</td>
</tr>
<tr>
<td>AAVCC+5</td>
<td>FB18</td>
<td>5.010</td>
<td>5.009</td>
<td>1</td>
<td>33</td>
</tr>
<tr>
<td>-5V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PLL</td>
<td>FB22</td>
<td>-4.988</td>
<td>-4.865</td>
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<td>34</td>
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<tr>
<td>TDM</td>
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<td>-4.989</td>
<td>-4.977</td>
<td>12</td>
<td>37</td>
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<tr>
<td>FIL</td>
<td>FB17</td>
<td>-4.991</td>
<td>-4.953</td>
<td>38</td>
<td>33</td>
</tr>
<tr>
<td>SPT</td>
<td>FB21</td>
<td>-4.993</td>
<td>-4.771</td>
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<td>32</td>
</tr>
<tr>
<td>DAC</td>
<td>FB16</td>
<td>-4.997</td>
<td>-4.992</td>
<td>5</td>
<td>31</td>
</tr>
<tr>
<td>3.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC3_LVDS</td>
<td>FB23</td>
<td>3.438</td>
<td>3.435</td>
<td>3</td>
<td>35</td>
</tr>
</tbody>
</table>
On board#2 two reworks were performed:

- The 500mA ferrite bead loaded in FB21 (digitizer segment) was interchanged with the 3A ferrite bead loaded in FB19 (VTTL1). The voltage drop over FB21 (digitizer segment) was reduced to 5mV, and the drop over FB19 (VTTL1) increased to 85mV. The voltage drop over the VTTL1 ferrite bead now exceeds the 50mV requirement.

- The 500mA ferrite bead loaded in FB22 (ECL PLL segment) was interchanged with the 3A ferrite bead loaded in FB24 (VTTL2). The voltage drop over FB22 (ECL PLL segment) was reduced to 4mV, and the drop over FB24 (VTTL2) increased to 110mV. Again, the voltage drop over the VTTL2 ferrite bead now exceeds the 50mV requirement.

The reworks to the power segment ferrite beads reduces the ECL/LVPECL supply ferrite bead voltage drops to acceptable levels, however, they increase the voltage drops on the TTL segments. To keep the VTTL segment supplies within 50mV of the main supply bus voltage, the final design should use at least 1A rated beads (this may require using 0804 or 1206 SMT-packages, instead of the 0603 packages used by the 500mA beads). The TTL voltage drops on the evaluation boards are acceptable for testing (they are still within 2-percent of 5V).

For the rest of this document, it is assumed that after power up, and after a board reset, that the following steps are performed:

- Set the digitizer and correlator AD9501 delays to zero.
- Enable the TDM logic and select divide-by-16 mode (64MHz)
- Select 64MHz output clock (this is the default)
- Enable the LVDS drivers
- Pulse the threshold DAC reset line to ensure the thresholds are all reset to 800h (-0.5V), then set the plus and minus threshold voltages and load them. For example, set the plus threshold to 400h (-0.25V), and the minus threshold to C00h (-0.75V).

When interfacing and testing with the correlator boards, the quantization state counters can be used to determine the optimal threshold voltages. The suggested voltages should be the starting point for the search.
4 Clock generation and control

4.1 Reference delay control

The Analog Devices AD9501 is a programmable delay chip [2]. An external resistor and (optional) capacitor give a delay of

\[
\text{delay} = t_{PD} + \left( \frac{\text{DAC code}}{256} \right) \cdot t_{DFS} = t_{PD} + \delta \cdot (\text{DAC code})
\]

where the propagation delay, \( t_{PD} \) is typically 25ns, \( \delta \) is the delay slope in ps/bit, and the full-scale delay, \( t_{DFS} \), is set by the external resistor and capacitor to

\[
 t_{DFS} = 3.84 \cdot R_{SET}(C_{\text{EXT}} + 8.5\text{pF}).
\]

For a 1kΩ external resistor and no external capacitor, the full-scale delay should be \( t_{DFS} = 32.64\text{ns} \), and the delay per bit \( \delta = 127.5\text{ps/bit} \). The output pulse has a typical width of 7.5ns.

Figure 1 shows the delay characteristics of the AD9501 in the correlator and digitizer sections of the evaluation board #1 (fully loaded). Figure 2 shows the waveforms obtained from the correlator AD9501. For the correlator AD9501, at a delay setting of zero, the delay to the rising edge, \( t_{PD} \), is 14.0ns and the pulse width is 10.5ns. At a delay setting of 0xFF, the delay to the rising edge \( t_{PD} + t_{DFS} \) is 48.7ns and the pulse width has reduced to 6.9ns. A least squares fit the delay characteristic in Fig. 1(a) gives a delay per bit of 135.5ps/bit, slightly larger than the value calculated using the data sheet equations. The pulse width had an average value of around 8.5ns, consistent with the data sheet value. The propagation delay of 14ns was well below the data sheet typical value of 25ns.

Measurements on the digitizer AD9501 in Fig. 1(b) show results similar to those obtained from the correlator AD9501. The delay per bit of 145.8ps/bit is slightly larger in this case. The clock phase control algorithm will have to be tolerant of slight slope differences in the AD9501s. Fig. 1 shows that the delay to the rising edge is the most linear. Delay to the falling edge is slightly non-linear due to the change in pulse width with delay setting.

The AD9501 uses a poor naming convention for the latch enable signal. The signal is referred to as LATCH, however, it is actually an active low signal. The initial system controller code implemented this signal as an active high signal, so caused a number of weird effects during the initial debug phase (since the latch was being left transparent).

Testing and calibration of the AD9501 delay using the phase detector circuit (see Figure 36) gave a calibrated delay of 148.1ps/bit for the digitizer section AD9501. This delay is within 3ps of the manual calculation performed using the oscilloscope, and confirms that the PLL is locking to the rising edge of the reference source. The AD9501 calibration using the phase detector circuit was performed in January, 2001. The oscilloscope measurements in this section were taken in June, 1999 (according to the dates on the scope captures). This shows that the AD9501 delays are constant with time.

Figure 13(a) shows how the AD9501 in the digitizer reference path can be used to shift the relative phases of the TDM output clock to the correlator clock. Also shown are the operation of the digitizer clock masking circuit and the TDM synchronization controls.
Figure 1: Delay characteristics of the AD9501. The data sheet specifies the delay to the rising edge as linear, with a typical device propagation delay of 25 ns and an incremental delay (slope) of 127.5 ns per bit. The measured characteristic of the AD9501 in the correlator section shown in (a) has a propagation delay of 14.0 ns, and a slope of 135.5 ps/bit, while the AD9501 in the digitizer section shown in (b) has a propagation delay of 13.5 ns, and a slope of 145.8 ps/bit.

Figure 2: Waveforms from the AD9501 measurements in Fig. 1(a) for; (a) a delay setting of 0x00 and (b) a delay setting of 0xFF. Channel 2 shows the waveform on TRIGGER (pin 3), while channel 3 shows the OUTPUT (pin 10). The oscilloscope is triggered off the 16 MHz reference. The delay and pulse width are measured using the $\Delta t@lv$ function with measurements made at 2 V.
Figure 3: The 3.3V clamping action of the BusSwitch circuit in the correlator reference signal path. The 4.39V output of the AD9501 is clamped to 3.11V.

4.2 Correlator reference clamp

The correlator SY89421 PLL is configured in LVPECL mode. The 16MHz reference routed to the PLL is converted to LVPECL using a 100LVEL22 LVTTL-to-LVPECL converter. Since this converter is not 5V tolerant, the output of the AD9501 delay is clamped to 3.3V using a BusSwitch [21]. Figure 3 shows that this circuit operates correctly. The supply VTTL3 = 4.94V at the diode, the drop over the diode was 0.55V, and the BusSwitch VCC = 4.39V. The on drop of the FET switch (∼1.3V) then limits the output voltage to 3.11V. See references [20,24] for more details.

An alternative method of generating the 4.3V VCC for the BusSwitch is to use a 4.3V Zener diode [25]. The circuit can be seen in the correlator schematic [9] clock delay page, and in the digitizer baseboard schematic [10] on the LVDS clock delay and clamp page. The 150Ω bias resistor in the zener clamp circuit generates the required Zener bias current of \((5V - 4.3V)/150Ω \approx 5mA\). A through-hole 4.3V Zener and a single bit BusSwitch was used to test this new clamping circuit configuration. The circuit clamped the output voltage, but to 3.6V not 3.3V. Since the Zeners used in the correlator board are different, we will need to confirm that the waveform is clamped to 3.3V (3.6V is a little close to the maximum voltage allowed for 3.3V devices). Either choosing a lower voltage Zener (say 4.0V) or changing the series current limiting resistor should allow the tuning of the clamp voltage to 3.3V. The characterization curves for the Zeners imply that a lower bias current (larger bias resistor) reduces the Zener voltage.

An alternative to using the BusSwitch to clamp the 5V signal to 3.3V is to use a 5V tolerant 3.3V buffer. Subsequent to designing with the BusSwitch, Fairchild introduced the TinyLogic line of devices in tiny SOT-23/SC-70 packages. The choice between whether to use a BusSwitch or TinyLogic device is arbitrary for this clamping operation, however in a situation where a delay or current drive is required, then a TinyLogic device may be a good solution. For example, on the correlator revision B.2 boards the NC7WZ16 2-bit buffers [7] were used to fanout the JTAG controls to improve the waveforms relative to observations on the revision A.3 boards.
4.3 Phase locked-loop (PLL)

When the digitizer evaluation boards were first powered-up, it was observed that the PLL would often not lock and would be stuck with a 1.39GHz output. If a PLL was locked and the VCO control voltage was probed with a voltmeter, then the PLL would unlock. The following discusses two problems with the digitizer evaluation board PLL configuration.

During power-up, the system controller FPGA does not drive any control lines until it is configured. During this tri-stated stage, the SY89421Vs see a control bit reading of S[5..1] = 10111 (since undriven TTL inputs float to a voltage that is read as high). With a 16MHz reference, this unintentional control word inserts a 40-bit feedback counter. Given the external divide-by-four counter, the requested VCO frequency is $160 \times 16MHz = 2560MHz$. This request is far above the VCOs maximum of 1120MHz. The PLL unlocks and gets stuck at 1.39GHz. Once at this frequency, there are two possibilities for getting the PLL to lock at the desired frequency.

The first method that was experimentally determined to lock the PLLs (most of the time) was to program the feedback counters to $\times1$ and $\times1$, this forces the PLLs to unlock at the bottom end of the frequency range, and from there the PLLs should lock to the requested output frequency.

The second method, recommended by Synergy engineers, places a clamping diode (a Schottky barrier diode) in the feedback path of the PLL filter. With the clamping diode in place, if the PLL unlocks and the control voltage heads toward the top end of the VCO range, then the control voltage is clamped to 0.3V above the VCO bias. The clamped control voltage is below the unlocked and stuck 1.39GHz control voltage, and from the clamped voltage, the PLL can be programmed and locked. Testing of the new PLL configuration with a spectrum analyzer showed that the addition of the clamping diode brings up the reference spur levels considerably. These spurs were reduced by increasing the loop filter order. Figure 4 shows the passive components required to implement the second order filter along with the diode and series resistor. The diode orientation is such that it will conduct for control voltages larger than the bias voltage plus 0.3V. A clamp diode in a reverse orientation could be used to clamp control voltages at 0.3V below the bias voltage. However this clamp was not needed, since if the PLL control settings cause the PLL to unlock at the bottom end of the VCO range, it will lock correctly when programmed with valid control settings.

To reduce the chance that the PLL will see incorrect control voltages, the control signals should have pull-up/down resistors that set a default power-up PLL setting. If the setting needs to be changed, then the system controller can drive the control signals to the desired state after it is configured.

On 6/24/99 during a visit to Synergy, engineers there indicated that the cause of the PLL clamping at a high frequency was in part due to the feedback counter. Apparently the feedback counter output voltage swing is too low when the PLL gets to too high an operating frequency. At that point, the feedback signal at the phase detector is essentially gone, so the PLL continues to drive toward the highest frequency possible. A newer revision of the chip hopes to solve this problem. Interestingly enough, a feedback clock is still visible at the PLL Fin pin at unlocked frequencies, so the Synergy explanation does not match the test results. The clamping diode does however fix the problem.

To determine the optimal component choice for the second order loop filter used in the SY89421V PLL, a separate PLL analysis document was written [13]. This document contains PLL theory and a detailed analysis of the Synergy SY89421V and SY89429A PLLs. The PLL document also shows test results for the Motorola MC12430 (similar to the SY89429A) and fractional-N synthesizers from National Semiconductor.
Figure 4: The SY89421V with a 2nd order filter and clamping diode. The SY89421V contains a phase-frequency detector (PFD) with a charge-pump output. The charge-pump output current pulses are filtered by the PLL filter to generate a control voltage. The clamping diode (Schottky barrier diode) stops the control voltage from exceeding 300mV above the bias voltage, and stops the VCO from getting stuck at 1.39GHz. Appropriate clamping diodes are MACOM/AMP MA4CS102A, HP HSMS-2820, or an equivalent Schottky barrier diode with a threshold voltage of 300mV (eg. Digikey carries Zetex diodes).
Figure 5: Correlator PLL waveforms. Trace A shows the reference Rin, trace B shows the feedback signal Fin, and trace C shows Fout. The two screen captures are for HFout/Fout settings of (a) 512MHz/128MHz, and (b) 512MHz/64MHz.

4.4 Reference and PLL timing

Figures 5 and 6 show the PLL waveforms on the correlator PLL (LVPECL-levels) and digitizer PLL (ECL-levels) on the digitizer evaluation board. These figures match the timing diagrams in the engineering specification. The measured timing parameters of interest are:

- Fout/Fin delay due to fanout and divide-by-four. For the digitizer PLL this was 1.1ns (100EL11 plus 100EL33 delay). For the correlator PLL this was 1.8ns (100LVEL14 plus 100LVEL33 delay). Both delay measurements are close to the data sheet estimates.

- Rin to Fout delay. For the digitizer PLL with HFout at 1024MHz, the delay is 4.3ns, and with HFout at 512MHz, the delay is 500ps. For the correlator PLL with HFout at 1024MHz, the delay is 3ns, and with HFout at 512MHz, the delay is 250ps. This parameter is not specified in the SY89421V data sheet.

- HFout to Fout. For the digitizer PLL, there was no discernable delay between the HFout and Fout signals. HFout is not measurable on the correlator PLL. This parameter is not specified in the SY89421V data sheet.

The Rin to Fout delay change with PLL HFout setting can be seen in Figure 6.
Figure 6: Digitizer PLL waveforms. Trace A shows the reference $R_{in}$, trace B shows the feedback signal $F_{in}$, trace C shows $F_{out}$, and trace D shows $HF_{out}$. The four screen captures are for $HF_{out}/F_{out}$ settings of (a) 1024MHz/128MHz, (b) 1024MHz/64MHz, (c) 512MHz/128MHz, and (d) 512MHz/64MHz.
4.5 Digitizer PLL TTL-to-(TTL-5V) translation circuit

Probing of the digitizer PLL control voltages showed that low control voltages were not translated to -5V, but were clamped at a diode drop below ground. Discussions with Pericom engineers indicated that this was due to input protection diodes on the BusSwitch. Pericom engineers had previously indicated that the use of a BusSwitch in this circuit would work.

The concept for the -5V translation logic is sound, however, a dual-supply analog switch is required. The clamp diodes on a dual-supply switch will not be activated by the circuit. The Pericom PS391/PS392 are appropriate dual-supply analog switches [22, 23].

Figure 7 shows the modified circuit using the dual-supply Pericom PS392 analog switch. Note that the figure shows the use of a normally-open (N.O.) switch. The PS391 is a normally-closed (N.C.) switch. If the PS391 is used, then there is an inversion between the input control signal and the control signal at the PLL. This inversion can easily be taken care of by the system controller code. Reworks on the digitizer evaluation boards used PS391 switches (and the digitizer PLL controls were inverted by the system controller). The digitizer board can use either the PS391 or PS392 or equivalent devices.

The digitizer evaluation board used 10kΩ pull-downs on the digitizer PLL controls to generate the logic low voltage (-5V). This pull-down had to be reduced to 500Ω, due to the high input leakage current of the SY89421V. The SY89421V maximum input leakage current is specified as 0.3mA, this would generate 3V across a 10kΩ pull-down. This exceeds the SY89421V specified TTL maximum input low voltage (V_{IL}) of 0.8V, in fact it exceeds the minimum input high voltage of (V_{IH}) of 2V so would be interpreted as a logic high control voltage.
The PS391/PS392 switches have an on resistance of 16Ω (typical), the input high leakage current of the SY89421V is 20µA, so the current through the switch when it is closed will be dominated by the current through the pull-down resistor. The logic high voltage should be approximately −16/516 × 5 = −0.16V. This voltage will be interpreted correctly as a logic high by the SY89421V.

With the PS391 rework circuit in place, the high voltage measured was -0.10V, while the low voltage was -4.83V (with the SY89421V supply voltage $V_{EE}$ at -4.93V). The logic low voltage of 0.10V above the (nominal) -5V supply across the 500Ω pull-down implies an input leakage current of 0.10V/500Ω = 0.2mA, which is less than the 0.3mA PLL maximum rating.

4.6 Correlator clock fanout

The MPC949 fanout chip is used to distribute clocks to the correlator FPGAs. In the correlator system, the input is an LVPECL signal, or a 33MHz signal (for debug purposes). On the evaluation board, the input is a 3.3V clamped version of the 16MHz reference, or a LVPECL signal from the PLL, or a LVPECL signal from the PLL converted to LVTTL. The four output banks on the MPC949 can be programmed to output a signal at the same frequency as the input, or at half the input frequency. This section confirms the programming features of the MPC949, while the next section confirms the data sheet indications that the MPC949 is capable of driving dual source terminated transmission lines.

The MPC949 LVTTL power segment and the PLL LVPECL power segment are generated from a common 3.3V backbone. Since the LVPECL signal is referenced to the 3.3V supply, it is necessary that both power segments have the same nominal 3.3V level (similar voltage drops across their segment power filters). On the “CMOS Clock Fanout” schematic p11, there is an 100EPT23/100EL23L LVPECL-to-LVCMOS converter connected to the VLVPECL power segment, its 3.3V supply was at 3.41V with a noise level of 87mV_{pp} or 15mV_{rms}. The MPC949 supply, $VCC3_{FIL}$, was at 3.41V with a noise level of 95mV_{pp} or 20mV_{rms}. The power supply levels and noise are acceptable.

The 3.3V clamp works correctly. The 16MHz reference and the control signals are all clamped to around 3.0V. The TCLK0 (clamped 16MHz ref.), TCLK1 (LVTTL converted PLL output), and PCLK (PLL LPCLK_{FOUT} signal) clock input signals all have the correct HIGH and LOW level voltages.

The power up defaults for the MPC949 (once the system controller is loaded) are; use the LVPECL clock as the input reference, output banks A, B and C fanout at the same frequency as the input, and output bank D is at half the input frequency. This initial state was confirmed, i.e., $FANOUT\_D[6..0] = 0011000b = 18h$. The ability to program each of the control bits was also confirmed. The output waveforms frequencies and state (enabled/disabled) change appropriately relative to the control bit settings.

4.7 Correlator clock terminations

The correlator clock fanout output waveforms can be observed through a cable with a 50Ω terminated oscilloscope, however, the voltage swing observed will be half height (due to the source and end termination). Observing the output waveforms with a 1MΩ oscilloscope input does not yield particularly nice waveforms, as the cable capacitance unduly affects the waveforms. The least intrusive way (the best way) to observe the outputs is to probe the SMB connectors with a FET probe (making sure a short ground probe is used). This gives the most realistic output, i.e., the waveforms will be similar to those at the clock inputs of the FPGAs on the final correlator board.

Figures 8 and 9 show the output waveforms from the MPC949 fanout chip for its default configuration with a 128MHz LVPECL input. The oscilloscope traces show the rise (10-90%) and fall (90-10%) times, frequencies, and amplitudes of the output waveforms. The measurements were taken with the timebase of channel 2 at 0.2µs (to get enough data for statistics) and then channel A is a zoomed version of a portion of the data. All waveforms were probed with a 1GHz, 10:1, 1MΩ/1.8pF.
Figure 8: Correlator clock waveforms (from the MPC949 fanout chip). (a) LTCLK\_CORR\_A0 (dual source terminated), (b) LTCLK\_CORR\_A1 (dual source terminated), (c) LTCLK\_CORR\_A8 (single source terminated), and (d) LTCLK\_CORR\_A9 (no source termination). If (d) is terminated in 50Ω (by an oscilloscope input), then the waveform is similar to (a)–(c). All waveforms were probed with a 1GHz, 10:1, 1MΩ/1.8pF FET probe.
Figure 9: Correlator clock waveforms (from the MPC949 fanout chip). (a) LTCLK_CORR_B0 (dual source terminated), (b) LTCLK_CORR_B1 (dual source terminated), (c) LTCLK_CORR_B2 (single source terminated, with an additional 15pF load), and (d) LTCLK_CORR_B2 at 128MHz. All waveforms were probed with a 1GHz, 10:1, 1MΩ/1.8pF FET probe.
FET probe (using a Le Croy LC584AXL oscilloscope with AP020 FET probes). Slightly faster rise and fall times were observing using a Tektronics TDS820 with P6207 4GHz, 100kΩ, 0.4pF FET probes. The data sheet values for rise and fall time are (max) 1ns for transitions from 0.8V to 2V [17]. Measurement of the rise and fall time for this specification yielded values about 40% of the 10-90% measurements. The parameter r@level on each of the figures is the rise time from 0.8V to 2V. The measured rise and fall times in Figures 8 and 9 are all less than the specified maximum of 1ns (the exception is the unterminated clock, which was expected).

Figures 8(a) and (b) and Figs. 9(a) and (b), are the waveforms from dual source terminated transmission lines (two drivers, four waveforms). Figures 8(c) and 9(c) are driven from single source terminated drivers. Figures 8(a) and (b) versus (c) clearly demonstrate that the MPC949 can drive a dual source terminated transmission line with no degradation in rise or fall time. Figure 9(c) has a 15pF load (in addition to the probe) to simulate the worst case loading of an FPGA clock pin. Figure 9(d) shows the waveform loaded with 15pF at 128MHz. The clock waveform still has a full voltage swing, however, the voltage never quite discharges to zero before the rising edge begins. The observed rise/fall time of 1.8ns is about 20% of the waveform period. A rise/fall time of 0.8ns would have been ideal, however, the waveform in Figure 8(d) should be adequate. Reducing the source resistance from 43Ω to 33Ω (a value on-hand) increased the voltage swing of the waveform and improved the rise/fall times slightly. On the final correlator board, the clock pins will be available as test points. The rise time observed at an FPGA can be tuned during final debug by reducing the source resistance if necessary. Reducing the source termination may increase under/overshoot at an output frequency that is divide-by-two, hence, any tuning should check both clock frequencies (i.e., both MPC949 output settings) for acceptable waveforms.

The signals LTCLK\_FANOUT0 and LTCLK\_FANOUT1 are routed to the LVDS translator and phase detector CPLD respectively. Probing the waveforms on U27.22 and U38.41 showed good quality 128MHz waveforms at the receiver end of the relevant transmission line. The load capacitance of the LVDS transceiver and the Cypress CPLD are 5pF and 8pF respectively, i.e., about half that of an FPGA clock input. The waveforms observed with these real loads had much faster transitions than the simulated 15pF load.

Figure 10 shows waveforms captured from a correlator board prototype (revision A.3). The observed risetimes of the FPGA clocks are similar to the digitizer evaluation board clock with the 15pF load (to simulate a correlator FPGA). The 128MHz clocks could be improved by reducing the source termination resistors.
Figure 10: Correlator board clock waveforms. (a) The four traces (measured at the correlator FPGA test points, and triggered off trace A) are: FPGA#0 A clock (64MHz), FPGA#0 B clock (128MHz), FPGA#3 A clock (64MHz), and FPGA#3 A clock (128MHz). The rise times of the four traces are 2.6ns, 2.3ns, 2.2ns, and 2.1ns respectively. These rise times are similar to the 2.5ns (64MHz) and 1.8ns (128MHz) measured on the digitizer evaluation board (where the FPGA load was simulated with a 15pF load). (b) The four traces (measured at the LVDS transceiver pins, and triggered off LVDS#0 clock) are: FPGA#0 LVDS transmit clock at 64MHz, FPGA#3 LVDS transmit clock at 64MHz, FPGA#0 LVDS transmit clock at 128MHz, FPGA#3 LVDS transmit clock at 128MHz. The rise times in (b) are 1.82ns, 1.82ns, 1.42ns, and 1.43ns respectively.
Figure 11: Digitizer clock pulse masking operation. The solid line shows that the clock masking circuit fails to operate on some occasions (once in 40 samples here). The dashed line shows that if the phase detector voltage is checked each time the pulse mask is asserted, then operation of the circuit can be confirmed or retried.

4.8 Digitizer clock pulse masking

The clock pulse masking circuit correctly shifts the TDM output clock by one digitizer clock period. However, Figure 11 shows that the pulse masking circuit fails intermittently at around the 2% level. There are two possible causes for this failure; the system controller is not sending the pulse mask signal, or the 1GHz state machine is failing. Simulations of the system controller show no reason for it to fail. Scope captures of the clock disable pulse are required to determine if the clock disable pulse is either not being generated, or perhaps not disabling the clock (due to a timing violation).

Figure 11 shows that failure in this circuit is tolerable, as read-back of the phase detector voltage can be used to confirm the success of a pulse mask command. If the phase detector voltage does not change, then the command can be retried.

The digitizer clock was reduced to 512MHz to see if that removed the pulse masking problem. Failures of the circuit were still observed, however, the failure rate dropped to less than 0.5% of the time. Clearly there is a marginal timing parameter that is the cause of this problem.

Figure 12 shows waveforms captured from the pulse masking circuit (while operating at 512MHz). The waveforms closely match those predicted in the engineering specification. The clock disable pulse follows the rising edge of the input clock by about 500ps, and the delay of the clock through the 100EL15 is also about 500ps.

Figure 13(b) shows how the digitizer clock pulse masking circuit can be used to shift the relative phases of the TDM output clock to the correlator clock. Also shown are the operation of the AD9501 and TDM synchronization controls.
Figure 12: Digitizer clock pulse masking circuit operation. (a) shows the input clock (U45.12) and pulse mask clock disable pulse (U45.15), (b) shows the pulse mask disable pulse (U45.15) and the output clock (U45.8) with a clock period deleted. These waveforms were taken with a Tektronics TDS 820. (c) shows the same three waveforms taken using the lower input bandwidth Le Croy LC584AXL.
Figure 13: Output clock phase control. The AD9501 can introduce phase steps of around 140ns/bit (with a 1kΩ delay setting resistor). (a) shows delays of approximately 2ns, 1ns, and 500ps. (b) shows that assertion of the digitizer clock pulse masking circuit deletes a digitizer clock period, increasing the relative phase between the correlator and digitizer clocks by one digitizer clock period, i.e., 0.977ns (for 1024MHz). (c) shows how the assertion of the TDM synchronization control deletes a TDM clock period, i.e., 1.95ns. Trace 2 is the correlator fanout clock, Trace 3 is the TDM output clock. Both clocks are at 64MHz and were measured at the input to the phase detector. The oscilloscope was configured in analog persistence mode so that the previous TDM output clock traces would remain displayed.
5 Digitizer

5.1 Reference and threshold voltages

Figure 14 shows the noise present on the SPT7610 ladder references. The decoupling for these references was incorrectly placed on the underside of the PCB. The vias through the PCB are inductive, and therefore have a high impedance at the 1024MHz clock frequency, so the decoupling does nothing. Figure 15 shows the reduction in noise due to the addition of 100pF decoupling directly to the SPT7610 reference pins. The final digitizer design will use high-quality, high-frequency decoupling for the reference decoupling, so the noise should be reduced further still. The noise remaining in Figure 15 is still due to inadequate decoupling, and probably due to rework wire pickup, and ‘scope probe pickup.

SPICE simulation of the OP491 reference voltage generator logic showed that programming range of each voltage would be limited due to the limited current sink/source ability of the OP491. This limit was reduced further still by the operation of the OP491 with 0V and -5V supplies. The circuit arrangement was copied from the SPT7610 application note. Programming of the DAC7624/OP491 reference voltages on the digitizer evaluation board confirmed the SPICE simulation results. The use of 0V and -5V supplies for the OP491 does not appear to be supported in the data sheet, and when the OP491 was replaced with the OP462, the circuit failed to work! The OP462 obviously will not operate with a 0V and -5V supply (the OP162 SPICE model confirms this), both ±5V supplies are required if negative output voltages are desired.

SPICE simulations of the OP191 -1V reference generator showed that the circuit was unstable (there was no phase margin in the circuit loop gain). Figure 16 shows measurements of the -1V reference on the digitizer evaluation board. When the board is powered-up, or the DAC7624 is reset, the reference voltages are all reset to -500mV. Figure 16(a) shows that the -1V reference oscillates at about 360kHz after reset. Figure 16(b) shows that the -1V reference will also oscillates at about 1.4Hz after transitions on the minus reference. SPICE simulation of this circuit predicts the 1.4MHz oscillation (the oscillation occurs at 1.6MHz in the SPICE model).

Figure 17 shows the transient response of the OP462 threshold/reference voltage generator. The transient response closely matches that of the SPICE model shown in the engineering specification. The noise on the waveforms is due to inadequate decoupling of the reference voltages, rework wire pickup, and probably some ‘scope pickup (although a very short ground probe connection was used). Figure 18 shows the ‘dc-sweep’ response of the OP462 reference voltage generator. The triangle waveform on each reference was generated by programming one reference at a time from 0V to -1V and then back to 0V in 100mV steps. Again, the noise on the waveforms is due mainly to inadequate decoupling of the reference voltages, and rework wire pickup. Figure 18(c) shows some variation in the -1V reference depending on the level of the minus reference. It is not clear why the feedback loop is not correctly holding this point at -1V.

5.2 Input buffering

The digitizer evaluation board buffers the input to the SPT7610 digitizer using a Mini-circuits ERA-6SM dc to 4GHz RF amplifier [16]. The results of Section 13.4 confirm that the RF amplifier is required on the input, and that it correctly buffers the RF input. For the final digitizer boards, a 3dB pad on the input is recommended.

The dc-linearity tests performed in Section 13.2 requires that the RF input be removed or turned-off. RF power can be reduced by either switching the RF amplifier input, or digitizer input to a 50Ω termination, or by removing power from the RF amplifier. The first option requires a wideband RF switch that can handle the 0dBm to 13dBm input power, while the second option requires that the RF amplifier has high off-isolation. Both options require a control signal.
Figure 14: OP491/OP191 threshold/reference voltage generator and -1V reference noise waveforms. (a) plus reference (-250mV nominal), (b) zero reference (-500mV nominal), (c) minus reference (-750mV nominal), and (d) -1V reference. The noise is obviously 1024MHz clock noise. These traces were taken with the oscilloscope triggered off the 16MHz reference. This noise is due to inadequate decoupling at the reference pins on the digitizer.
Figure 15: OP491/OP191 threshold/reference voltage generator and -1V reference noise waveforms, with an additional 100pF decoupling on each of the digitizer reference voltage pins. (a) plus reference (-250mV nominal), (b) zero reference (-500mV nominal), (c) minus reference (-750mV nominal), and (d) -1V reference. The clock noise is reduced significantly relative to Figure 14. These traces were taken with the 'scope triggered off the 16MHz reference.
Figure 16: OP191 -1V reference voltage oscillations. (a) after reset, when all of the reference voltages are set to -500mV, a 360kHz oscillation (2.8μs period) is observed, and (b) transients on the minus reference generate a 1.3MHz oscillation. These oscillations are due to inadequate phase margin in the reference generator loop gain. These oscillations are not synchronous with the 1024MHz clock noise, and they are not due to aliasing by the digital oscilloscope. A similar oscillation is predicted by a SPICE model of the circuit.

Figure 17: OP462 threshold/reference voltage generator transient responses. (a) rising edges, and (b) falling edges. The threshold were each individually stepped ±250mV about their nominal settings, while the other two references were set to their nominal values. The noise on the waveforms is due to inadequate decoupling.
Figure 18: OP462 threshold/reference voltage generator ‘DC-sweeps’. (a) plus reference, (b) zero reference, and (c) minus and -1V reference. The threshold were each individually stepped from 0V to -1V and then back to 0V in 100mV steps, while the other two references were set to their nominal values. The -1V reference shown in (c) shows some variation with the minus threshold setting. The noise on the waveforms is due to inadequate decoupling.
5.3 Output data control
The operation of the digitizer TEST, MINV, and LINV controls was confirmed.

5.4 Digitizer timing
Figure 19 shows the digitizer timing at 512MHz. Relevant observations from this figure are:

- Figure 19(a) shows that the clock-to-output delay of the input clock to DRA is about 1ns. The timing of DRB (not shown) was similar to DRA, but inverted. The clock-to-output delays are consistent with the SPT7610 data sheet typical delay of 1.15ns.

- Figure 19(b) shows the relative timing of the falling edge of DRA to the transition of DA[5:4]. The transition on DA[5:4] is 320ns after the transition on DRA, hence the clock-to-output delay of the data is 1.32ns. This delay is 420ps larger than the data sheet typical delay of 900ps.

- Figure 19(b) exposes an error in the SPT7610 data sheet. Figure 1 in the data sheet shows the timing for input clock edge N is a rising edge transition on data-ready A and a transition on the data-A bank. However, Figure 19(b) shows that it is the falling edge of DRA that occurs after the same clock edge as a data transition, i.e., the SPT data sheet has DRA and DRB inverted in its Figure 1. Figure 2 in the data sheet is correct, however, for the digitizer board the TDM logic timing was calculated using the SPT Figure 1. To correct for downstream timing errors, the clock buffers for the TDM circuits need their clock inputs swapped.

- Figure 19(c) shows the relative timing of DRA to DB[5:4]. As expected, the eye-patterns of the two data banks are spaced by one digitizer clock period.

- Figure 19(d) shows the timing of the falling edge of DRA to the transition of DA[5] while the digitizer is in test pattern mode. In test mode, the clock-to-output delay is slightly larger than when digitizing an input RF. The 480ps delay observed implies a clock-to-output delay of 1.48ns for the test pattern. This is over 0.5ns larger than the typical data delay stated in the SPT data sheet.

- Figure 19(e) shows the timing of the rising edge of DA[5] to what should be the rising edge of DB[5]. The SPT7610 loaded on board#1 has a faulty test pattern generator. Board#2 showed the correct relationship between DA[5] and DB[5].

Figure 20 shows the timing tests performed at 1024MHz. Similar tests were performed on the digitizer evaluation board#2. The SPT7610 test pattern worked correctly on board#2. Tables 6 and ?? show the measured timing results for the digitizer and TDM logic on board#1 and board#2. These timing results are discussed in more detail in following sections.

Figure 19(b) and (c), and Figure 20(b) and (c) show an interesting potential problem. While probing the DRA and DA[5:4] signals with the digitizer digitizing the RF, there is a lot of ‘fuzz’ on the output data-ready and data signals. This ‘fuzz’ is not due to poor probe grounding, as a probe held on DRA will observe Figure 19(b) (or Figure 20(b)) trace 1 when the digitizer is digitizing the RF and Figure 19(d) (or Figure 20(d)) trace 1 when the digitizer test mode is selected. This means that this ‘fuzz’ is generated internal to the digitizer and is not due to capacitive coupling of the RF signal around the package pins. Both noise inputs and CW input showed a similar level of ‘fuzz’. Actually, even with no RF input (and no RF buffer amplifier) this ‘fuzz’ was present. However, the autocorrelation tests in Section 13.4 show that this ‘fuzz’ does not seem to affect the measured spectra.
Figure 19: Digitizer timing at 512MHz. (a) shows the input clock and the 1ns clock-to-output delay to DRA. DRB is similar to DRA, but inverted. (b) shows the relative timing of the falling edge of DRA to the transition of DA[5:4] (about 320ns). (c) shows the relative timing of DRA to DB[5:4]. As expected, the eye-patterns of the two data banks are spaced by one clock period. (d) shows the timing of the falling edge of DRA to the transition of DA[5] while the digitizer is in test pattern mode. (e) shows the timing of the rising edge of DA[5] to what should be the rising edge of DB[5]. The digitizer loaded on board#1 has a faulty test pattern generator. Board#2 showed the correct relationship between DA[5] and DB[5]. See the text for comments on the ‘fuzz’ seen in (b) and (c).
Figure 20: Digitizer timing at 1024MHz. (a) shows the input clock and the 1ns clock-to-output delay to DRA. DRB is similar to DRA, but inverted. (b) shows the relative timing of the falling edge of DRA to the transition of DA[5:4] (about 350ns). (c) shows the relative timing of DRA to DB[5:4]. As expected, the eye-patterns of the two data banks are spaced by one clock period. (d) shows the timing of the falling edge of DRA to the transition of DA[5] while the digitizer is in test pattern mode. (e) shows the timing of the rising edge of DA[5] to what should be the rising edge of DB[5]. The digitizer loaded on board#1 has a faulty test pattern generator. Board#2 showed the correct relationship between DA[5] and DB[5].
6 Data time division multiplexing (TDM)

6.1 TDM mode

The MODE control switches between demux-by-4 and demux-by-8 mode on the E445s. The control signal operates correctly. Correlation testing shows that the TDM logic operates correctly for demux-by-16 data (64MHz).

TODO: The correct operation of the TDM circuit for demux-by-8 data (128MHz data) needs to be confirmed, by autocorrelating data for this mode (requires a 128MHz clock correlator configuration).

6.2 TDM reset and synchronization

Figure 21 shows the TDM reset timing for a TDM clock frequency of 256MHz (i.e., a 512MHz digitizer clock). The measured timing shows how TDM_RESET is synchronized to the rising edge of DRA to generate TDM_RESET_A, and how TDM_RESET_B is generated by registering TDM_RESET_A with the rising edge of DRB, i.e., with the falling edge of TDM_RESET_A. The observed clock-to-output delay of the 100EL30 of about 700ps is within the data sheet specification.

The eight 100E445 serial-to-parallel converters all come out of reset with the correct relative timing. To test the correct operation of TDM reset exhaustively, the correlator board phase detector was used to confirm that the relative phase between its 128MHz clock and the digitizer evaluation board CLK/4-A and CLK/4-B clocks showed a consistent phase difference after reset (CLK/4 clocks were used, as the digitizer output clock select multiplexer does not have an option for selecting CLK/8-A). This loop also placed the digitizer in test mode and read back the test pattern. This test confirmed the operation of TDM reset; there was always a consistent voltage difference (absolute value, since the phase detector has a positive and negative slope), and the two possible valid test patterns were read back consistently.

The TDM synchronization control, TDM_SYNC, works correctly. Figure 13(c) shows how the TDM_SYNC control can be used to shift the relative phases of the TDM output clock to the correlator clock. Also shown are the operation of the AD9501 and digitizer clock pulse masking controls.

Figure 22 shows the results of the TDM circuit operation. Figure 22(a) shows the delay between the two clocks as measured by the oscilloscope at the input to the phase detector CPLD (using Δt@lv(2,3), between 1.5V points on the rising edges of the two input channels). Figure 22(b) shows the phase measured by the oscilloscope (using Δphase(2,3) between 1.5V points on the rising edges of the two input channels), and Figure 22(b) shows the phase detector response in volts. The phase detector response is the ADC0808 result. This voltage was confirmed using the oscilloscope to read the voltage on the ADC0808 input pin. The ADC0808 showed no glitches during sampling of the phase detector voltage (as was observed on the AD7828 inputs on the correlator prototypes).
Figure 21: TDM reset timing at 256MHz (512MHz digitizer clock). TDM_RESET (U29.2) is synchronized to the rising edge of DRA (U29.3) to generate TDM_RESET_A (U29.16), and TDM_RESET_B (U29.12) is generated by registering TDM_RESET_A with the rising edge of DRB, i.e., with the falling edge of TDM_RESET_A. The observed clock-to-output delay of the 100EL30 is about 700ps. All traces were captured by triggering off TDM_RESET_A. The reflection visible on TDM_RESET_B is due to the measurement being performed at the source. This reflection is not present on the 100E445 pins.
Figure 22: TDM synchronization control operation. (a) shows that each time TDM\(_{\text{SYNC}}\) is pulsed, the relative delay between channels increases by a TDM clock period (two digitizer clock periods). (b) shows relative phase measured between the two reference clocks. After 4 assertions of the TDM\(_{\text{SYNC}}\) control, the clocks are 180° out-of-phase. (c) shows the phase detector output voltage. The reference trace was the correlator clock (from the fanout chip), while the delayed clock was the TDM clock. Measurements were obtained at 64MHz. (a) measurements were obtained using \(\Delta t_{\text{iv}}(2,3)\), between 1.5V points on the rising edges of the two input channels, (b) measurements were made using \(\Delta \text{phase}(2,3)\) between 1.5V points on the rising edges of the two input channels.
6.3 TDM timing

During the debug of the digitizer evaluation board, it was observed that the digitizer data-ready clocks were inverted with respect to the SPT7610 data sheet and that the observed clock-to-output data delay was close to 500ps larger than expected (the data sheet only states a typical delay, but since this is close to half a clock period, it is rather excessive). The timing for the TDM logic is based on the timing from the data sheet, so with the clock error and additional data delay, there is the potential for data setup or hold violations at the TDM logic.

Tables 5, and 6, and Figures 23, 24, and 25 show the measured TDM timing on board#1. Similar measurements were obtained on board#2. Table 5 and Figure 23 show the TDM timing on board#1 with the clock error. The inversion of the SPT7610 data-ready clocks causes a 140ps hold violation on one of the 100E445 inputs. This hold violation does not occur for the test pattern, as it was observed to have a 160ps larger clock-to-output delay than the digitized RF input (see Table 6). Table 6 shows that the measured clock-to-output delay of the SPT7610 is on the order of 500ps larger than the data sheet typical delay of 900ps. This additional delay reduces the setup time, and increases the hold time, available at the 100E445 serial-to-parallel converters.

Figure 23 shows that DB[4] (U5) is the only 100E445 input to have a hold violation. Figure 26 shows the autocorrelation lags and spectra of a 250MHz low-pass filtered noise source. This figure indicates that although the measured timing indicates a hold violation (relative to the data sheet requirement), that this hold violation may not be occurring. The ‘fuzz’ visible in the lag response is mainly composed of a 512MHz component. Figure 27 shows the autocorrelation lags and spectra of a 250MHz low-pass filtered noise source after the clock inversion has been corrected. The improvement in both the lag response and the spectral response (the shape improves and the 512MHz component is gone) indicates that the hold violation was affecting the digitizer output data. Figure 28 shows the output of board#2 with the clock error, noisy threshold voltages, and no RF amplifier present. Comparison of this spectra to that in Figure 27 shows the improvement due to the board reworks. Figure 32 shows the timing at the output of the TDM logic.

If strange lag and spectra results are observed from a digitizer board, a possible test to distinguish errors in the TDM-A and TDM-B logic is: using a 128MHz noise source, write a correlator HDL configuration that contains two autocorrelators, one that processes even samples (TDM-A data) and one that processes odd samples (TDM-B data). The resulting lags/spectra are effectively 128MHz noise sampled at 256MHz. The lags/spectra measured should be identical, within the expected statistical variation (since the lags/spectra were generated with different samples).

The data-ready clocks from the SPT7610 digitizer are fanned out to the 100E445 serial-to-parallel converters using 100EL14 1:5 clock fanout buffers. The 100EL14 has a multiplexer on its input, one channel accepts a differential clock (this is the input we used), while the other input accepts a single-ended clock. The data sheet for the 100EL14 does not give a maximum clock frequency for the single-ended input. Prior to inverting the differential clock inputs (to correct the clock flip error), the data-ready clock was routed to the single-ended input, and the multiplexer control driven such that the single-ended clock was selected. The output clocks of the 100EL14 were then inverted. The quality of the output waveforms was insufficient for the correlator board to read back the correct number of quantization counts. This test demonstrated that the single-ended input of the 100EL14 does not operate at 512MHz.

6.4 Supply tolerance/timing errors

During initial testing with the digitizer in test mode, the ECL supply on board#1 was lowered to around -4.5V. At that voltage (which is still within specification for 100-series ECL), the TDM logic operation was incorrect. The TDM outputs should have been static voltages, however, they showed glitching signals. At lower supply voltages, device delays are increased, and due to the digitizer data-ready output clock sense error noted in the engineering schematic and described in the last section, this test exposed a timing error (most likely a hold violation).
Table 5: Digitizer evaluation board#1. TDM setup and hold times/margins at 1024MHz with the digitizer clock flip error.

<table>
<thead>
<tr>
<th>Description</th>
<th>Part</th>
<th>Data sheet</th>
<th>Min (ps)</th>
<th>Typ (ps)</th>
<th>Max (ps)</th>
<th>Margin (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100E445 serial-input setup time (DA5)</td>
<td>U3</td>
<td>-100</td>
<td>1000</td>
<td>1100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100E445 serial-input setup time (DA4)</td>
<td>U1</td>
<td>-100</td>
<td>1180</td>
<td>1280</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100E445 serial-input setup time (DB5)</td>
<td>U7</td>
<td>-100</td>
<td>1180</td>
<td>1280</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100E445 serial-input setup time (DB4)</td>
<td>U5</td>
<td>-100</td>
<td>1420</td>
<td>1520</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100E445 serial-input hold time (DA5)</td>
<td>U3</td>
<td>450</td>
<td>710</td>
<td>260</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100E445 serial-input hold time (DA4)</td>
<td>U1</td>
<td>450</td>
<td>480</td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100E445 serial-input hold time (DB5)</td>
<td>U7</td>
<td>450</td>
<td>550</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100E445 serial-input hold time (DB4)</td>
<td>U5</td>
<td>450</td>
<td>310</td>
<td>-140</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figures 29, 30, and 31 show the lags and spectra for a 250MHz low-pass filtered noise source for ECL supply voltages of -4.2V, -4.1V, and -4.0V (measurements were made after correcting the digitizer clock error). The lags and spectra were observed to be correct for ECL supply voltages below -4.3V. An interesting point to note about Figure 31 is that it looks very similar to the output of the correlator when using a 500MHz bandwidth filter (except for the additional noise). Due to this potential confusion, debugging of problem digitizer boards should be performed with a narrower and filter than the Nyquist rate of the digitizer.
Table 6: Digitizer evaluation board#1. Measured digitizer and time-demultiplexing (TDM) logic device timing, and TDM setup and hold margins at 1024MHz. (Setup and hold times are calculated for digitization of the RF input. Test mode decreases the setup time, and increases the hold time, by 160ps due to the different measured clock-to-data ready delays).

<table>
<thead>
<tr>
<th>Description</th>
<th>Part</th>
<th>Data sheet</th>
<th></th>
<th>Measured</th>
<th>Margin</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPT7610 clock-to-data ready clock delay</td>
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<td>1150</td>
<td>1000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SPT7610 clock-to-data delay - test mode</td>
<td>U48</td>
<td>750</td>
<td>900</td>
<td>1050</td>
<td>1320</td>
</tr>
<tr>
<td>SPT7610 clock-to-data delay - RF input</td>
<td>U48</td>
<td>750</td>
<td>900</td>
<td>1050</td>
<td>1480</td>
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<tr>
<td>SPT7610-to-100EL14 trace delay (DRA)</td>
<td>U30</td>
<td></td>
<td>700</td>
<td></td>
<td></td>
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<tr>
<td>SPT7610-to-100EL14 trace delay (DRB)</td>
<td>U28</td>
<td>500</td>
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<td></td>
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<tr>
<td>SPT7610-to-100E445 trace delay (DA5)</td>
<td>U3</td>
<td>920</td>
<td></td>
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<tr>
<td>SPT7610-to-100E445 trace delay (DA4)</td>
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<tr>
<td>SPT7610-to-100E445 trace delay (DB5)</td>
<td>U7</td>
<td>560</td>
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<tr>
<td>SPT7610-to-100E445 trace delay (DB4)</td>
<td>U5</td>
<td>500</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>100EL14 propagation delay (DRA)</td>
<td>U30</td>
<td>580</td>
<td>680</td>
<td>780</td>
<td>750</td>
</tr>
<tr>
<td>100EL14 propagation delay (DRB)</td>
<td>U28</td>
<td>580</td>
<td>680</td>
<td>780</td>
<td>750</td>
</tr>
<tr>
<td>100E445 serial-input setup time (DA5)</td>
<td>U3</td>
<td>-100</td>
<td>0</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>100E445 serial-input setup time (DA4)</td>
<td>U1</td>
<td>-100</td>
<td>200</td>
<td>300</td>
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<tr>
<td>100E445 serial-input setup time (DB5)</td>
<td>U7</td>
<td>-100</td>
<td>200</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>100E445 serial-input setup time (DB4)</td>
<td>U5</td>
<td>-100</td>
<td>410</td>
<td>510</td>
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<tr>
<td>100E445 serial-input hold time (DA5)</td>
<td>U3</td>
<td>450</td>
<td>1700</td>
<td>1250</td>
<td></td>
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<tr>
<td>100E445 serial-input hold time (DA4)</td>
<td>U1</td>
<td>450</td>
<td>1450</td>
<td>1000</td>
<td></td>
</tr>
<tr>
<td>100E445 serial-input hold time (DB5)</td>
<td>U7</td>
<td>450</td>
<td>1450</td>
<td>1000</td>
<td></td>
</tr>
<tr>
<td>100E445 serial-input hold time (DB4)</td>
<td>U5</td>
<td>450</td>
<td>1200</td>
<td>750</td>
<td></td>
</tr>
<tr>
<td>100E445 (cascaded) setup time</td>
<td>U2,4,6,8</td>
<td>-100</td>
<td>900</td>
<td>1000</td>
<td></td>
</tr>
<tr>
<td>100E445 (cascaded) hold time</td>
<td>U2,4,6,8</td>
<td>450</td>
<td>850</td>
<td>400</td>
<td></td>
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<tr>
<td>100E445 clock-to-sout delay</td>
<td>U1-U8</td>
<td>800</td>
<td>1150</td>
<td>1000</td>
<td></td>
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<tr>
<td>100E445 clock-to-clk/4 or clk/8 delay</td>
<td>U1-U8</td>
<td>1100</td>
<td>1550</td>
<td>1300</td>
<td></td>
</tr>
<tr>
<td>100E445 clock-to-q delay</td>
<td>U1-U8</td>
<td>1500</td>
<td>2100</td>
<td>1750</td>
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<tr>
<td>100EL57 propagation delay</td>
<td>U60</td>
<td>360</td>
<td>560</td>
<td>500</td>
<td></td>
</tr>
<tr>
<td>100EL11 propagation delay</td>
<td>U61</td>
<td>190</td>
<td>265</td>
<td>340</td>
<td>400</td>
</tr>
<tr>
<td>100ELT25 propagation delay</td>
<td>U59,U62</td>
<td>1700</td>
<td>3600</td>
<td>2400</td>
<td></td>
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<tr>
<td>GL1LSM300S analog delay-i-trace delay</td>
<td>U71</td>
<td>3000</td>
<td>4300</td>
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<td>100393 propagation delay</td>
<td>U65-U68</td>
<td>2300</td>
<td>4800</td>
<td>3100</td>
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<tr>
<td>DS92LV090 driver propagation delay</td>
<td>U23,U24</td>
<td>600</td>
<td>2200</td>
<td>2200</td>
<td></td>
</tr>
<tr>
<td></td>
<td>U27,U28</td>
<td></td>
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</tbody>
</table>
Figure 23: Time-demultiplexer (TDM) timing at 1024MHz (with digitizer data-ready clock inversion error). These four figures show the waveforms on the CLK and SIN pins of the appropriate 100E445s, and the available hold time. (a) DA[5] (U3) 860ps, (b) DA[4] (U1) 600ps, (c) DB[5] (U7) 580ps, and (d) DB[4] (U5) 360ps. The setup and hold times of the 100E445 are -100ps and 450ps respectively. The inversion of the data-ready clock introduces a hold violation on DB[4].
Figure 24: Time-demultiplexer (TDM) timing at 1024MHz (with digitizer data-ready clock inversion error fixed). These four figures show the waveforms on the CLK and SIN pins of the appropriate 100E445s, and the available hold time. (a) DA[5] (U3) 1700ps, (b) DA[4] (U1) 1450ps, (c) DB[5] (U7) 1450ps, and (d) DB[4] (U5) 1200ps. The setup and hold times of the 100E445 are -100ps and 450ps respectively. Fixing the clock inversion error corrects the hold violation on DB[4].
Figure 25: Time-demultiplexer (TDM) timing at 1024MHz (with digitizer data-ready clock inversion error fixed). These four figures show the waveforms on the CLK and SIN pins of the cascaded 100E445s, and the available hold time. (a) DA[5] (U4) 850ps, (b) DA[4] (U2) 950ps, (c) DB[5] (U8) 850ps, and (d) DB[4] (U6) 950ps. The setup and hold times of the 100E445 are -100ps and 450ps respectively. All cascaded 100E445s have adequate timing margin.
Figure 26: Board#1 response for a 250MHz low-pass filter, with the clock flip error.

Figure 27: Board#1 response for a 250MHz low-pass filter, with the clock flip error fixed.
Figure 28: Board#2 response for a 250MHz low-pass filter, with no fixes (i.e., the board has the clock flip error, noisy threshold voltages, and no RF amplifier on the input).

Figure 29: Board#1 response for a 250MHz low-pass filter, with the ECL supply reduced to -4.2V.
Figure 30: Board#1 response for a 250MHz low-pass filter, with the ECL supply reduced to -4.1V.

Figure 31: Board#1 response for a 250MHz low-pass filter, with the ECL supply reduced to -4.0V. The only correlated lag is lag zero.
7 Digitized data output clock

7.1 Multiplexer

The digitized data is routed over LVDS to the correlator boards. The LVDS cable carries a clock signal so that data can be either clocked into a FIFO at the receiving end, or so that clock phases in the system can be aligned. The clock that is routed with the digitized data is selectable as; the PLL Fout signal, the TDM-A CLK/4 signal, and the TDM-B CLK/4 and CLK/8 signals. The operation of the multiplexer was confirmed. The 100EL57 multiplexer output signal quality was excellent at both 64MHz and 128MHz. Figure 32 shows the clock and data output from the TDM logic. The clocks observed at the 100EL57 output were similar to those in the figure.

7.2 Fanout

The 100EL11 1:2 fanout output (100ELT25 ECL-to-TTL translator input) was excellent at 64MHz and 128MHz. However, the TTL output of the 100ELT25 displayed poor rise/fall times on both the single source and the dual source terminated transmission lines. Figures 32 and 33 show the eye-patterns of the clock and data as measured for various points between the output of the TDM logic, and the LVDS connector. Figure 33(d) and (e) show that the output of the TTL translator does not fully discharge to 0V before swinging high again.

The data sheet for the 100ELT25 used during the design of the board did not state a maximum operating frequency for the device, however, more recent data sheets state a maximum frequency of 100MHz for this device. The 100EPT25 is a newly released 3.3V ECL/LVECL to LVTTL translator. This device has a maximum operating frequency of 265MHz, however, it operates from a LVTTL supply voltage of 3.3V (which was not planned to be used on the final digitizer module board). Figure 34 shows the output clock of a dual-source terminated 100EPT25 (U59 reworked) versus a single-source terminated 100ELT25 (U62). This test confirms that the 100EPT25 operates at 128MHz, and should be used on the final digitizer module.

7.3 Analog delay line

Table 6 shows that probing from the output of the 100ELT25 ECL-to-TTL translator to the input of the LVDS transceiver gives a delay of 4300ns. Since the delay line is part of a much longer source terminated transmission line, probing at the input and the output of the delay line does not give you two square-waves shifted in time. Figure 35 shows the clock waveforms measured at the input to the analog delay line. The clock waveforms were measured at three frequencies; 32MHz, 64MHz, and 128MHz. The 32MHz clock shows that the round-trip delay (the step in the waveform) from the input of the delay line to the end of the transmission line (delay line plus trace to load) is about 6ns. This indicates that the delay line is about 3ns long. The round-trip waveforms at 64MHz cancel each other out, while the waveforms at 128MHz show little distortion. The waveforms measured at the LVDS transceiver could have been nicer. For the final digitizer baseboards, a TinyLogic 3.3V buffer should be placed at the output of the delay line to drive the transmission line to the LVDS transceiver (the delay lines will be several inches from the LVDS transceivers). Point-to-point transmission lines (i.e., single source terminations) should provide for an end termination option.
Figure 32: Time-demultiplexer (TDM) demultiplexed output timing (eye-patterns) at 1024MHz digitizer clock. (a) TDM-by-16 timing (64MHz): 100E445 CLK/8, Q2 and, (b) TDM-by-8 timing (128MHz): 100E445 CLK/4, Q2. Both measurements are from U3.
Figure 33: TTL and LVDS eye-patterns at TDM-by-16 (64MHz) and TDM-by-8 (128MHz). TDM-by-16 eye-patterns: (a) ECL-to-TTL translator output, (b) LVDS input, and (c) LVDS output. TDM-by-8 eye-patterns: (d) ECL-to-TTL translator output, (e) LVDS input, and (f) LVDS output.
Figure 34: TDM TTL output clock; 100EPT25 (top trace) versus 100ELT25 (bottom trace). The 3.3V 100EPT25 shows much cleaner rise and fall times. Both clocks were measured at the source.

Figure 35: Analog delay line clock waveforms; 32MHz, 64MHz, and 128MHz. The clocks were measured at the input to the delay line. The 32MHz clock shows that the round-trip delay (the step in the waveform) from the end of the transmission line is about 6ns. This indicates that the delay line is about 3ns long.
8 Digitized data level translation

8.1 ECL-to-TTL

The eye-patterns at the top of Figure 33 show that the 100393 ECL-to-TTL translators operate correctly with data at clock rates of 64MHz and 128MHz (the fastest data toggles is half the clock rate, i.e., 32MHz or 64MHz).

8.2 TTL-to-LVTTL

The eye-patterns in the middle of Figure 33 show that the BusSwitch 3.3V clamps operate correctly with data at clock rates of 64MHz and 128MHz.

8.3 LVTTL-to-LVDS

The eye-patterns at the bottom of Figure 33 show that the LVDS transceiver drivers operate correctly with data at clock rates of 64MHz and 128MHz.

There were a couple of errors with the LVDS section that were found during debugging: data bus bits 10 and 11 are interchanged at the inputs to the LVDS transceivers due to a schematic error. The decal numbering for the LVDS transceivers on the underside of the board are wrong, i.e., they are incorrectly numbered in a clockwise direction and pin 1 is in the wrong place (the chips were however loaded correctly).

8.4 Digitized data output timing

The eye-patterns at the bottom of Figure 33 show the clock and data timing at the LVDS connector. The falling edge of the clock is close to the center of the data eye. Comparing these measured eye-patterns with those predicted in the engineering specification shows that the measured timing delays are close to the typical parameters, i.e., the uncertainty in the engineering specification due to data sheet timing ranges is conservative relative to what is observed on the board. The LVDS waveforms look similar to the waveforms predicted at the output of the ECL TDM logic, hence the delay of the clock and data through the logic translations from ECL to LVDS has been well matched. This matching can be seen by comparing the TDM output timing in Figure 32 to the LVDS signals at the bottom of Figure 33.

9 Monitor/control digitizer

The monitor analog-to-digital converter is a National Semiconductor ADC0808 [18]. The system controller generates a 1MHz clock for the converter by dividing the 33MHz system clock by 32. An 8-bit conversion takes approximately 64 clock cycles, i.e., $64\mu s$. In addition to the conversion time, the analog mux must be allowed to settle for $2.5\mu s$ (if the ADC0808 has just changed channels). There were some timing problems with the initial GDA system controller code and the sense of the AD9501 latch enable control was inverted. Once the system controller code was rewritten, the monitor ADC correctly read back the monitor point voltages and the phase detector output. Figure 44 shows the interface waveforms. These waveforms match the simulation waveforms in the engineering specification.

The $64\mu s$ conversion time of the ADC0808 could have been a problem in the final correlator system, so on the correlator boards (and eventually the digitizer boards), the ADC0808 is replaced with an Analog Devices AD7828 flash converter. This ADC has a conversion time of $2.5\mu s$. 
9.1 Temperature sensors (REF-02, AD22100)

The voltages from the temperature sensors were measured with a voltmeter and the monitor ADC, the values obtained were consistent. The temperature measured from the AD22100 was reasonable. However, 'scope traces of both temperate sensor outputs showed that there was kickback on the ADC0808 analog inputs during conversion. This kickback is due to the switching of the input analog multiplexer internal to the ADC0808. This kickback needs to be eliminated by buffering the output of the temperature sensor with a fast settling-time op-amp.

The REF-02 data sheet specifies the temperature response for a $V_+ \text{ of } 15V$. We are using a $V_+ \text{ of } 12V$. To convert the REF-02 output voltage to a temperature requires the correct voltage-to-temperature conversion. Using the 15V transfer function, the board reading of 655mV corresponds to a temperature of 37-degrees C. This is higher than the actual board temperature. Analog Devices were contacted for this information and they indicated that they don not recommend using the REF-02 as a temperature sensor. The correlator and digitizer baseboards need to have an AD22100 added to replace the TEMP output of the REF-02 (the REF-02 remains as the 5V reference).

9.2 Power supply monitor points

The four power supplies monitored; 5V, -5V, 3.3V, and -2V were measured with a voltmeter, and then with the monitor ADC. The measurements were consistent.

10 Clock phase detector

The phase detector has three input clocks; the TDM output clock (this is the clock that is also transmitted with the output data), the correlator clock (from the fanout chip), and the clock received from the LVDS transceivers. The output of the phase detector CPLD is low-pass filtered and sampled by the ADC0808 analog-to-digital converter. The voltage read by the ADC0808 represents a phase difference between the clocks. The digitizer clock pulse masking circuit and the TDM logic generate known phase steps in the relative clock phases, these controls can be used to calibrate the phase detector voltage response (in units of Volts/ns). Once the phase detector is calibrated, the AD9501 phase detector response can be calibrated in terms of Volts/bit, then using the previous phase detector calibration in units of Volts/ns, the AD9501 delay can be determined; in ps/bit.

The TDM clock fed to the phase detector logic is driven by a source terminated 100ELT25 ECL-to-TTL translator. This device does not output a reasonable waveform at 128MHz (even with a reduced source termination). The waveform is very triangular, and does not reach ground. A similar issue was observed with the TDM clocks driven to the LVDS transceivers, and test SMB. These clocks were generated using a dual-source terminated 100ELT25. If the LVDS transceivers are configured in loopback mode, the 'received' LVDS clock observed at the phase detector CPLD has the correct voltage swing, however, the mark-space ratio is not 50/50 due to the poor ECL-to-TTL translator waveform driving the transceiver.

Figure 36 shows the measured transfer function of the phase detector and digitizer AD9501. The calibration of the phase detector and AD9501 transfer functions were performed with a 64MHz clock (divide-by-16 mode). The clock period at 64MHz is 15.625ns, and the delay range of the digitizer AD9501 is approximately 37ns (from Fig. 1(b)), i.e., about 2.4 clock periods.

Figure 36 shows that the maximum voltage recorded on the phase detector output (pin 37 of the Cypress CPLD) was around 3.5V. The slope of the digitizer clock masking circuit response and the slope of the TDM synchronizer response should then be 3.5V/15.625\text{ns} = 224mV/\text{ns}. A least-squares fit to each of the measured data sets gave slopes of 219mV/\text{ns} for the digitizer clock masking circuit response and 217mV/\text{ns} for the TDM synchronizer response. The measured AD9501 response was 32.3mV/bit (compare to the 28.6mV/bit predicted in the engineering specification). This slope
Figure 36: Phase detector and AD9501 calibration. The digitizer clock pulse masking circuit (× symbol every 0.977ns) and the TDM synchronization control (○ symbol every 1.95ns) are used to calibrate the phase detector voltage response as 218mV/ns (the slope of the rising edge of the transfer function). The slope of the AD9501 transfer function, 32.3mV/bit, is then converted to AD9501 delay of 148.1ps/bit by dividing by the phase detector response.

This automatically calibrated result is within 3ps of the manual measurement, shown in Figure 1, that was performed using an oscilloscope.

Figure 13 shows how the AD9501 in the digitizer reference path, the digitizer clock masking circuit, and the TDM synchronization controls were used to shift the relative phases between the reference clock (the correlator clock) and the TDM output. The traces in Figure 13 were measured at the input pins on the phase detector CPLD.

Figure 37 shows the waveforms obtained from the phase detector circuit with 64MHz clocks. The waveforms match the theoretical analysis performed in the engineering specification.
Figure 37: Phase detector transfer function and output waveforms. (a) Shows the measured phase detector transfer function with 64MHz clocks (15.625ns period). (b) to (f) show the waveforms in the circuit at the five phase delays annotated on (a); (b) 0°, (c) 90°, (d) 180°, (e) 270°, and (f) 360°. Channel A of the plots is the reference clock (from the digitizer section), B is the second clock (from the correlator section), C is the output of the phase detector, and D is the input to the monitor digitizer. Delays were introduced into the correlator clock (input B) by programming the correlator AD9501.
Table 7: Typical ECL levels for 100-series devices at 25° [15, p1-14].

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
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<tr>
<td>V_{IH}</td>
<td>Input HIGH voltage</td>
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<td>-880</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>V_{IL}</td>
<td>Input LOW voltage</td>
<td>-1810</td>
<td>-1475</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>V_{OH}</td>
<td>Output HIGH voltage</td>
<td>-1025</td>
<td>-880</td>
<td>mV</td>
<td>50Ω to -2V</td>
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<tr>
<td>V_{OL}</td>
<td>Output LOW voltage</td>
<td>-1810</td>
<td>-1620</td>
<td>mV</td>
<td>50Ω to -2V</td>
</tr>
</tbody>
</table>

11 Differential logic levels

11.1 ECL levels

The levels of ECL control signals and clocks on the board were all measured to have valid ECL levels. The signal quality of clock and data waveforms were also checked. Signal quality checks require a very short probe lead to the GND pin of the device being probed. Figure 38 shows the levels typical of 10- and 100-series ECL. Table 7 shows the levels for the 100-series devices used in the Digitizer Evaluation Board design.

11.2 LVPECL levels

Table 7 shows the levels for the 100-series devices used in the Digitizer Evaluation Board design. These voltages are translated to LVPECL voltages by adding the level of the nominal 3.3V supply. Hence, the tests in this section were measured relative to the 3.3V voltage at the device tested.

The LVPECL signals are all terminated in 50Ω to $V_{cc} - 2V$ by a 3-resistor network contained in a three terminal resistor pack. Since all of the LVPECL waveforms have the correct output levels and are all of good quality, these terminations operate correctly.

11.3 LVDS levels

The LVDS waveforms (for example the bottom trace in Figure 33) were all within Bus-LVDS specifications.
Figure 38: Typical ECL levels at 25° for 10- and 100-series devices [15, p1-14]. The voltages in parenthesis are for a x2 probe.
12 System controller

The system controller memory map control register operation was confirmed by probing the control signals on the board. This testing exposed a net naming error: during TTL-to-ECL conversion of the digitizer control signals on p28 of the schematic, the control signals \( \text{dig}_{[2:0]} \) contain a flip of control bits 2 and 0 on the output of the TTL-to-ECL translators. This error was corrected by interchanging the pin assignments for bits 0 and 2 on the FPGA.

The following sections document and confirm the operation of the system controller state machines.

12.1 Parallel port (EPP) interface

Figure 39 shows the waveforms obtained from the parallel port interface. The waveforms show that the PC parallel port drivers are much stronger than the drivers on the digitizer evaluation board. The acknowledge signal \( \text{waitN} \) is driven directly by the FPGA, while the address/data bus \( \text{ad}_{[7:0]} \) is driven by a 74F245 bidirectional buffer. During read cycles both \( \text{waitN} \) and \( \text{ad}_{[0]} \) show similar responses, with the FPGA typically driving the bus to a maximum of 2.75V, and the 74F244 driving the bus to 3.6V. The FPGA high level of 2.75V exceeds the data sheet guaranteed minimum of 2.4V [1]. Similar results were obtained on board#1 with the 3.3V FPGA. However, the 3.3V FPGA must have stronger drivers, as it drives the \( \text{waitN} \) control to 3.1V.

Figure 40 shows the waveforms obtained during an address write timeout. The EPP timeout is measured to be 40\( \mu \)s. The specified timeout in the SuperI/O data sheet is a minimum of 10\( \mu \)s [19]. After a timeout, status bit 0 gets set to 1. Reading the status register clears this bit. Address write timeouts can be used to detect the presence or absence of a board with a particular EPP ID. For example, if a board with EPP ID = 0 is attached to the parallel port, an address write of any address in the range 00h to 7Fh should not result in a timeout. Similarly, if a board with EPP ID = 1 is attached to the parallel port, an address write of any address in the range 80h to FFh should not result in a timeout.

Figure 41 shows the conditioning of the EPP acknowledge signal, \( \text{waitN} \). When chaining two digitizer evaluation boards on the same parallel port, it is not possible for them both to drive \( \text{waitN} \) continuously, as this would cause a driver conflict. To avoid a driver conflict, each digitizer evaluation board must only assert \( \text{waitN} \) high when it is selected, otherwise it must tristate the handshake. Trace B shows \( \text{waitN} \) continuously driven by an FPGA (illegal for board chaining) for comparison purposes. Trace C shows \( \text{waitN} \) driven high, then tri-stated. Trace D shows \( \text{waitN} \) driven high, driven low for 240ns, then tri-stated. Trace D closely matches the continuously driven trace and is the interface used in the system controller.
Figure 39: Parallel port (EPP) interface waveforms; (a) address write, (b) address read, (c) data write, and (d) data read. Address strobe and data strobe are asserted low for approximately 0.5 µs. Notice that the parallel port drivers are much stronger than the drivers on the digitizer evaluation board. The signals were probed at the dual DB25 connector on the board.
Figure 40: EPP address write timeout. The timeout is about 40μs. After a timeout, status bit 0 gets set to 1. Reading the status register clears this bit. The timeout waveforms are similar for address read timeouts, and data write/read timeouts.

Figure 41: EPP acknowledge, \textit{waitN}, conditioning. When chaining two digitizer evaluation boards on the same parallel port, each board can acknowledge (assert the handshake high) only when it is selected, otherwise the control must be tristated. Trace B shows \textit{waitN} continuously driven by an FPGA (illegal for board chaining) for comparison purposes. Trace C shows \textit{waitN} driven high, then tri-stated. Trace D shows \textit{waitN} driven high, driven low for 240ns, then tri-stated. Trace D closely matches the continuously driven trace and is the interface used in the system controller.
12.2 Programmable delay (AD9501) write timing

Figure 42 shows the waveforms obtained during a write to the AD9501. The rising edge of the latch enable pulse occurs approximately 100ns after the data is stable. This is more than adequate to meet the AD9501 2.5ns setup and hold time. The waveforms in Figure 42 closely match those of the control register simulation waveforms contained in the engineering specification.

12.3 Threshold voltages (DAC7624) read/write timing

Figure 43 shows the threshold voltage (DAC7624) write/read timing. Figure 43(a) shows a write to the DAC, and Figure 43(b) shows a read from the DAC. The write timing meets the required 0ns data setup time and 50ns write cycle pulse timing. During a read cycle, the data is valid before data strobe goes high. (c) and (d) show an expanded scale of data strobe and the data bus bit d[10] during a write and read of 400h to the plus threshold. Since the digitizer evaluation board does not have bus pull-ups/downs, during a write the bus discharges from 3.3V (3.3V FPGA) and during reads the bus discharges from 5V. The RC discharge on data bus bits d[7:0] can be removed by using the bus hold feature of the Cypress CPLD, bits d[11:8] cannot be helped. Ideally, the data bus should have had bus pull-ups and downs on it.

12.4 Monitor digitizer (ADC0808) read timing

Figure 44 shows the monitor/control digitizer (ADC0808) write/read timing. A write to a ADC0808 channel starts a conversion. Figure 44(a) shows the 1µs ALE and START pulses, with the rising edge of ALE leading the falling edge of START by the required 3µs settling time(4µs measured). (b) shows an expanded view of the conversion. A conversion is complete when EOC returns high. (c) and (d) show the read timing. During both writes and reads, the datastbN input is synchronized to the monitor clock, so the EPP write/read cycles are extended to 3.5µs and 4µs respectively.
Figure 43: Threshold voltage (DAC7624) write/read timing. (a) shows a write to the DAC, and (b) shows a read from the DAC. The write timing meets the required 0ns data setup time and 50ns write cycle pulse timing. During a read cycle, the data is valid before data strobe goes high. (c) and (d) show an expanded scale of data strobe and the data bus bit d[10] during a write and read of 400h to the plus threshold. Since the digitizer evaluation board does not have bus pull-ups/downs, during a write the bus discharges from 3.3V (3.3V FPGA) and during reads the bus discharges from 5V.

Figure 44(b) shows the RC discharge on the data bus after the ADC0808 has driven a bit high. This RC discharge can be removed by using the bus-hold feature of the phase detector CPLD, or by the addition of bus pull-ups/downs on the data bus.

Note that the waveforms in Figure 44 were taken from the board with the 3.3V FPGA. The control signals to the ADC0808 are then at 3.3V. This is less than the data sheet required minimum of 3.5V, however, the device functions correctly (for this board). Ideally, the control signals to the ADC0808 should have had pull-ups to 5V (consequently a 5V tolerant FPGA would be required). Also, p8 of AN-247 [26] indicates that the ADC0808 is only capable of driving one TTL load. However, the waveforms in Figure 44 shows that the device has no problems driving the data bus.
Figure 44: Monitor/control digitizer (ADC0808) write/read timing. A write to a ADC0808 channel starts a conversion. (a) shows the 1µs ALE and START pulses, with the rising edge of ALE leading the falling edge of START by the required 3µs settling time (4µs measured). (b) shows an expanded view of the conversion. A conversion is complete when EOC returns high. (c) and (d) show the read timing. ALE was used for triggering the 'scope to preserve the timing between AD0808 control signals.
Figure 45: Bus hold effect on write/read waveforms. Each figure shows datastbN on channel 2 and one of the bus bits d[7:0] on channel 2. (a) and (b) show a write to, and a read from, the DAC with bus hold disabled. (c) and (d) show a write to, and a read from, the DAC with bus hold enabled. With bus hold enabled, a logic high is held on the bus at about 3.4V. The write data waveforms are generated by a 3.3V FPGA.

12.5 Phase detector CPLD (CY37064) bus hold

The phase detector CPLD can perform a bus hold function, i.e., the CPLD can be configured to contain a weak latch on its I/O pins such that the I/O latches the last state of the bus [4–6, 8]. The phase detector CPLD is connected to the data bus bits d[7:0]. Figure 45 shows the effect of disabling and enabling the bus hold feature on the data bus. Enabling bus hold removes the data bus RC discharge effect by holding the bus in its last state. Since data bus bits d[11:8] are not connected to the CPLD, the data bus RC discharge effect is not able to be mitigated on these bits (see Figure 43(c) and (d)). Ideally, the data bus should have contained bus pull-ups and downs.


13 Testing with a correlator board

The final digitizer board will contain FPGAs for quantization state monitoring, autocorrelation, digital delay, and data fanout. There is a limited number of tests that can be performed with the digitizer evaluation board to confirm the digitizer and TDM logic operation, since the digitizers in the correlator system quantize the input signal so coarsely. To fully test the digitizer and TDM logic, interfacing with a correlator board is required. The correlator board FPGA receiving data from the digitizer evaluation board is configured as a digitizer board FPGA, i.e., it contains logic to perform digital delays and quantization state monitoring. Autocorrelation or cross-correlations were then performed by another FPGA.

This section contains the results of testing the digitizer evaluation board with a correlator board.

13.1 Test pattern mode

The simplest DC test for the digitizer and TDM logic is to read the time demultiplexed digitizer output when the digitizer chip is placed in test mode. In test mode, the digitizer outputs the alternating pattern: 01, 01, 10, 10. The TDM output word for this pattern is 5A5A5A5Ah or A5A5A5A5h (pulsing TDM_SYNC toggles between the two patterns). The pattern just described assumes that the bits are interpreted in terms of the correlator board 32-bit format, this is slightly different than the digitizer evaluation board output bus definition. The correlator board FPGA receiving the digitizer evaluation board data performs a remapping of the bit assignments. Section 8 in the ‘Digitizer Evaluation Board Engineering Specification’ contains more details.

Testing of both digitizer evaluation boards exposed a number of problems (not all of these problems were found at once, so they lead to multiple problems):

- Digitizer evaluation board bus bits 10 and 11 (magnitude bits 0 and 2 in the TDM word) are interchanged at the inputs to the LVDS transceivers (U27). This schematic error is corrected in the correlator board FPGA during the remap of digitizer bus bits to the expected correlator word format.

- Digitizer evaluation board #1 LVDS output bit 0 was stuck low (TDM sign bit 6), i.e., a single channel in the 9-bit transceiver U23 was stuck low. Resoldering the LVTTL input did not correct the problem, so the device was replaced.

- The SPT7610 data-ready clocks are inverted with respect to the data sheet timing diagrams.

- The SPT7610 on digitizer evaluation board #1 outputs an incorrect (complimented) test pattern on one of the output data banks, i.e., TDM A and TDM B output patterns are complimented with respect to each other, when they should be the same.

Once the bit flip was found, the test pattern read back from board #2 was correct. However, board #1 read 69694969h or 96969696h due to the SPT7610 pattern error, and the transceiver error.

The error with the SPT7610 test pattern lead to several debugging problems:

- An autocorrelation of this pattern results in the same quantization state fractional counts, and lag counts. Hence, it is not possible to detect this error from looking at the lag results.

- The problem lead to the discovery that the SPT7610 output data-ready clocks are complimented with respect to some of the diagrams in the data sheet. This lead to the assumption that the TDM logic was having setup or hold violations, and was reading one of the digitizer banks a clock cycle too late or early (and hence the bits in the TDM word for A and B were complimented with respect to each other). However, probing the clock/data at the 100E445 devices showed adequate setup and hold time even with the SPT7610 clocks left inverted. This observation was due to a larger than expected clock-to-output delay from the SPT7610.
that offset the fact that the clocks were inverted. Finally, probing the SPT7610 data outputs showed the error with the test pattern. Figures 19 and 20 show waveforms probed at the SPT7610 at 512MHz and 1024MHz.

To confirm that the SPT7610 digitizer and TDM logic is outputting the correct test pattern, the TDM output word must be read and checked to see that it is A5A5A5A5h or 5A5A5A5Ah.

13.2 DC tests

The threshold voltages on the SPT7610 are controlled by 3 channels of a DAC. The forth channel of the DAC is connected to the input of the digitizer and is used to offset the input signal to the center of the digitizer input range (since the input is ac-coupled). The use of a DAC for setting this input voltage instead of a simple voltage divider allows for dc testing of the digitizer.

Figure 46 shows a dc-sweep of the input offset voltage, $V_{\text{offset}}$, from -1V to 0V in 10mV steps on board #1 (the RF amplifier input was terminated in 50Ω to ground for this test). The four plots show the fractional counts obtained at each voltage setting. The plus, zero, and minus thresholds were set to -250mV, -500mV, and -750mV respectively. The transition between patterns occurs close to these voltages. The observed transition points are about 20mV above the threshold voltages. This offset voltage is due to offsets in the threshold voltage generator logic, and due to offsets internal to the SPT7610.

Figure 47 shows a dc-sweep performed on board #2. Board #1 was reworked to contain capacitors on the STP7610 threshold voltage pins, while board #2 has no additional capacitors. Comparison of this plot to Figure 46 shows the importance of the decoupling; the additional noise on the threshold voltages causes digitization pattern variations for input voltages near the threshold voltages.

When the dc-linearity test was performed on board #1 when the LVDS transceiver bit 0 was stuck low, it showed that the 1/16 of the 10 and 11 patterns were generating 00 and 01 patterns (since 1 bit of the TDM output was stuck low). For example, setting the offset voltage to -0.9V and reading the TDM output gave AAAA8AAAh (sign bit 6 stuck low), i.e., 15 patterns of 10, and one pattern 00. The dc-linearity test is useful for checking the TDM logic, and interconnect between the digitizer and correlator board.
Figure 46: DC linearity testing (board #1). The offset voltage is swept from -1V to 0V in 10mV steps. The four plots show the fractional counts. The plus, zero, and minus thresholds were set to -250mV, -500mV, and -750mV respectively. The transition between patterns occurs close to these voltages.
Figure 47: DC linearity testing (board#2). The digitizer evaluation board has inadequate decoupling on the threshold voltages. Board #1 was reworked to contain capacitors on the STP7610 threshold voltage pins, while board #2 has no additional capacitors. Comparison of this plot to Figure 46 shows the importance of the decoupling.
13.3 Threshold tests

Digital correlation for radio astronomy applications simplifies the correlator logic by coarsely digitizing the input signal. This simplification results in a loss in signal-to-noise, e.g., for a 2-bit digitizer and correlation of 2-bits with deleted inner products, the efficiency is 0.87 relative to a digitizer with an infinite number of bits. The correlator efficiency of 0.87 is achieved so long as the threshold voltages are set correctly.

For the 2-bit deleted inner product multiplication scheme, the optimal settings for the plus and minus threshold voltages are ±0.9σ volts where σ is the RMS voltage of the input noise waveform. When the threshold voltages are set correctly, the probabilities for obtaining the digitized patterns 10, 11, 00, and 01 are 0.18, 0.32, 0.32, and 0.18 respectively (where we are assuming a 2’s compliment digitizer output, as this is the scheme we use). The quantization state counters (implemented in an FPGA), and their corresponding fractional counts (total counts normalized to 1), are used to determine whether the threshold voltages are set correctly.

The probability density function (PDF) of a random Gaussian noise input is

\[ p(y) = \frac{1}{\sqrt{2\pi}} \exp\left(\frac{-y^2}{2\sigma^2}\right) \]  

and the cumulative PDF (integral of the PDF) is

\[ P(y) = \frac{1}{2} \left[ 1 + \text{erf}\left(\frac{y}{\sqrt{2}\sigma}\right) \right]. \]  

The PDF for a sinusoidal source is

\[ p(y) = \frac{1}{\pi \sqrt{1 - \left(\frac{y^2}{\sigma^2}\right)}} \]  

and the cumulative PDF is

\[ P(y) = \frac{1}{\pi} \sin^{-1}\left(\frac{y}{\sqrt{2}\sigma}\right) + \frac{1}{2}. \]

Figure 48 shows plots of the PDFs and cumulative PDFs.

The analysis to determine the optimal threshold voltage of 0.9σ volts can be found in [14]. Using (4) and \( y/\sigma = -0.9 \) gives 0.184 as the probability of signal occurring below the minus threshold, i.e., \( P_{10} = P(y < V_{\text{minus}}) = 0.184 \). Assuming that the zero threshold is set at the center of the PDF, the probabilities (expected fractional counts) of the digitizer patterns are:

- **10**: \( P_{10} = P(y < V_{\text{minus}}) = 0.184 \)
- **11**: \( P_{11} = P(V_{\text{minus}} < y < V_{\text{zero}}) = 0.316 \)
- **00**: \( P_{00} = P(V_{\text{zero}} < y < V_{\text{plus}}) = 0.316 \)
- **01**: \( P_{01} = P(y > V_{\text{plus}}) = 0.184 \)

To test the setting of the digitizer evaluation board threshold voltages, the LVDS output of the digitizer evaluation board is routed to a correlator board. The clock phases between the two boards are aligned, and the correlator board correlates the data. For the digitizer evaluation board tests, the first FPGA on the correlator board contained quantization state counters and a digital delay line.

For a correlation (integration) period of approximately 6.18ms (31CA4h counts at 33MHz), and a quantization state counter prescaler length of 2, the expected total number of counts from the
Figure 48: Digitizer input probability density functions (PDFs) and cumulative PDFs. (a), (b) random Gaussian noise and (c), (d) sinusoidal.

quantization state counters is $31CA4h \times 64/(33 \times 4)=18240h$ (where the correlator clock is 64MHz). After correlating the input signal, the total number of counts read from the quantization state counters should be 18240h (within a few counts). On the few occasions that this was not the case, the digitizer evaluation board needed to be reset.

To determine the offset voltages and amplitudes of the input signal referred to each of the threshold voltages, the following tests were performed:

- $V_{\text{plus}}$ test:
  set $V_{\text{zero}} = -500\text{mV}$, $V_{\text{minus}} = -750\text{mV}$, and sweep $V_{\text{plus}}$ from -500mV to 0V in 25mV steps.

- $V_{\text{zero}}$ test:
  set $V_{\text{plus}} = -250\text{mV}$, $V_{\text{minus}} = -750\text{mV}$, and sweep $V_{\text{zero}}$ from -750mV to -250mV in 25mV steps.

- $V_{\text{minus}}$ test:
  set $V_{\text{plus}} = -250\text{mV}$, $V_{\text{zero}} = -500\text{mV}$, and sweep $V_{\text{minus}}$ from -1V to -500mV in 25mV steps.

Figures 49 and 50 show the threshold voltage transfer functions (cumulative PDFs) as measured by this set of tests. Figures 49 also shows, as dashed lines, the changes in the fractional counts for
the individual bit patterns. Ideally the fractional counts for the thresholds away from the threshold being tested should not change, however currents in the digitizer input resistive ladder cause slight changes in the threshold voltage as seen internally by the digitizer comparators.

Figure 50(a) shows an overlay of all three threshold voltage transfer functions. For input random Gaussian noise, each of the three threshold voltages see their own version of the input signal; each with a slightly different RMS and offset voltage. The cumulative PDF of Gaussian noise in (4) modified to account for an offset voltage is

\[ P(v) = \frac{1}{2} \left[ 1 + \text{erf} \left( \frac{v - v_{\text{offset}}}{\sqrt{2}v_{\text{rms}}} \right) \right]. \tag{7} \]

This function can be linearized to

\[ \text{erf}^{-1} \left[ 2P(v) - 1 \right] = \frac{v - v_{\text{offset}}}{\sqrt{2}v_{\text{rms}}} \tag{8} \]

which is of the form \( y = mx + c \). Performing a least squares fit to the linearized data allows the extraction of \( v_{\text{rms}} = \frac{1}{\sqrt{2m}} \) and \( v_{\text{offset}} = -\frac{c}{m} \). Figure 50(b) shows the linearized transfer functions, while the parameters in (a) and dashed lines in (a) and (b) are the least-squares fit parameters and curves.

The RMS and offset parameters shown in Figure 50(a) are due to internal offsets in the digitizer. Probing the SPT7610 pins with an oscilloscope show that the threshold voltages are set within a few millivolts of the requested threshold. For example, if all three thresholds are set to -500mV (the digitizer midpoint), then one would expect only the patterns 10 and 01 to occur, however, a correlation with these threshold settings gives fractional counts of 0.28, 0.26, 0.15, and 0.30 for the patterns 10, 11, 00, and 01 respectively. Removing the RF input and performing a DC-sweep of the input gives the results in Figure 51. Again, we see that even though the threshold voltages are correct at the pins of the SPT7610, there must be internal offsets.

These offsets can also be seen in Figure 50(a). Looking at the data points for the overlayed plots at -0.5V, shows that there are still counts of 11 and 00. The offset parameters in Figure 50(a) are offsets in the input waveform (not the threshold voltage), i.e., the plus threshold sees an input waveform with a negative dc-offset relative to the nominal midpoint of -500mV, hence, the plus offset must be set to a lower voltage relative to what it would have been without this apparent offset in the input waveform. This leads to the interesting observation that for small input waveforms, \( V_{\text{plus}} \) can be set lower than \( V_{\text{zero}} \) and \( V_{\text{minus}} \) can be set higher than \( V_{\text{plus}} \). Even though correlation of low amplitude waveforms appears to operate correctly, the threshold voltage setting routine should fail for voltage that do not meet the following requirement:

\[ -1V \leq V_{\text{minus}} \leq V_{\text{zero}} \leq V_{\text{plus}} \leq 0V \tag{9} \]

If \( V_{\text{plus}} \) needs to exceed 0V or \( V_{\text{minus}} \) needs to be less than -1V, then the input waveform amplitude is too high. If \( V_{\text{minus}} \) needs to be set greater than \( V_{\text{zero}} \), or \( V_{\text{plus}} \) needs to be set less than \( V_{\text{zero}} \), then the input waveform amplitude is too small.
Figure 49: Threshold voltage transfer functions (noise input). Changing each of the threshold voltages results in a corresponding change in the fractional counts for each digitizer output pattern: (a) $V_{\text{plus}}$ threshold, (b) $V_{\text{zero}}$ threshold, and (c) $V_{\text{minus}}$ threshold. This figure shows that for input Gaussian noise, the fractional counts follow the cumulative PDF of Gaussian noise.
Figure 50: Estimation of noise input RMS and offset voltages. (a) Overlaying $V_{\text{plus}}$, $V_{\text{zero}}$, and $V_{\text{minus}}$ threshold transfer functions obtained with a random Gaussian noise input clearly show the erf-like cumulative PDF. (b) Linearizing the transfer functions allows the extraction of the RMS and offset voltage of the input signal as seen by the three threshold voltages. The extracted parameters are shown in (a).
Figure 51: DC sweep showing threshold voltage offsets. All three threshold voltages are set to -500mV (confirmed with an oscilloscope), however, the digitizer output patterns imply that $V_{\text{plus}} \approx -380\text{mV}$, $V_{\text{zero}} \approx -470\text{mV}$, and $V_{\text{minus}} \approx -560\text{mV}$. 
Figures 52 and 53 show the threshold voltage transfer functions (cumulative PDFs) as measured using a sinusoidal input (100MHz). Figure 53(a) shows an overlay of all three threshold voltage transfer functions. The cumulative PDF of a sinusoidal source, as shown in (6), modified to account for an offset voltage is

\[ P(v) = \frac{1}{\pi} \sin^{-1} \left( \frac{v - v_{\text{offset}}}{\sqrt{2}v_{\text{rms}}} \right) + \frac{1}{2}. \]  

This function can be linearized to

\[ \sin \left[ \pi (P(v) - \frac{1}{2}) \right] = \frac{v - v_{\text{offset}}}{\sqrt{2}v_{\text{rms}}} \]  

Figure 53(b) shows the linearized transfer functions, while the parameters in (a) and dashed lines in (a) and (b) are the least-squares fit parameters and curves.

A possible implementation of the threshold setting algorithm is one that first determines the offsets and RMS voltages relative to the three threshold voltages, and then sets the optimal threshold locations (for input noise) to

\[ V_{\text{plus}} = V_{\text{plus,offset}} + 0.9V_{\text{plus, rms}} \]
\[ V_{\text{zero}} = V_{\text{zero,offset}} \]
\[ V_{\text{minus}} = V_{\text{minus,offset}} - 0.9V_{\text{minus, rms}}. \]  

This algorithm would require stepping the threshold voltages over their respective 0.5V range, and performing a least-squares fit for parameter extraction. In addition, the least-squares fit requires a knowledge of the input cumulative PDF.

A more generic threshold setting algorithm is one that takes as input the required fractional counts. The algorithm then starts by setting the thresholds to their nominal locations, performs a correlation, and reads back the fractional counts. The fractional counts are compared to the required fractional counts, and if they do not match, the threshold voltages are adjusted appropriately and the sequence is repeated. If each threshold is adjusted in the manner of a binary search (large voltage steps initially, with decreasing step size), then the algorithm can be terminated when the fractional counts read back are within tolerance of the required fractional counts (the algorithm should also be terminated with an error if the step size gets too small).

Figure 54 shows the results of the threshold setting algorithm for a noise source and sinusoidal source. The thresholds were set such that the fractional counts were all 0.25. Correlations (6.18ms long) were then performed once every minute and the fractional counts recorded. Figure 54 shows the results for a 2 hour period for each source. The figure shows that the fractional counts are stable for many hours. The variation in lag 0 is to be expected (since the integration period was only 6.18ms), and the variation of lag 0 from unity is due to the threshold settings. The threshold setting algorithm may want to use the value of lag 0 (which can also be calculated from the 01 and 10 pattern fractional counts) to determine when the thresholds are set accurately.
Figure 52: Threshold voltage transfer functions (sinusoidal input). Changing each of the threshold voltages results in a corresponding change in the fractional counts for each digitizer output pattern; (a) $V_{\text{plus}}$ threshold, (b) $V_{\text{zero}}$ threshold, and (c) $V_{\text{minus}}$ threshold. This figure shows that for a sinusoidal source, the fractional counts follow the cumulative PDF of a sinusoidal source.
Figure 53: Estimation of sinusoidal input RMS and offset voltages. (a) Overlaying $V_{\text{plus}}$, $V_{\text{zero}}$, and $V_{\text{minus}}$ threshold transfer functions obtained with a sinusoidal source clearly show the inverse sin-like cumulative PDF. (b) Linearizing the transfer functions allows the extraction of the RMS and offset voltage of the input signal as seen by the three threshold voltages. The extracted parameters are shown in (a).
Figure 54: Threshold stability for a noise source and sinusoidal source. At the beginning of each test, the thresholds were set such that the fractional counts were all 0.25. Over a 2hr period, a 6.18ms correlation was performed once per minute, and the fractional counts and lag 0 counts were recorded. (a) and (b) show the fractional counts and lag 0 results for the noise source, while (c) and (d) show the results for the sinusoidal source.
Figure 55: Threshold counts versus frequency for a sinusoidal input. The thresholds were set at 200MHz for fractional counts of 0.25 for all four patterns. With a 200MHz sinusoid of 0dBm amplitude at the RF amplifier input (actually the source was at 3dBm, and the board had a 3dB SMA pad on the input), the plus, zero, and minus threshold voltages were -0.39V, -0.54V, and -0.58V respectively. The input was then swept from 10MHz to 1020MHz in 10MHz steps and a correlation was performed at each frequency. The plot displays the fractional counts recorded. The digitizer clock frequency was 1024MHz, so frequencies above 512MHz are aliased.

To determine the bandpass characteristics of the digitizer, a sinusoidal input source was swept from 10MHz to 1020MHz. Figure 55 shows the results of setting the threshold voltages at 200MHz to obtain fractional counts of 0.25 for all four bit patterns, and then reading the fractional counts for the swept frequencies. If the input amplitude decreases at higher frequencies, then a consequent increase in the bit patterns 00 and 11 would be observed. The similarity between the counts from 10MHz to 500MHz to those from 500MHz to 1020MHz indicates that the input RF amplifier is maintaining the signal amplitude. Figure 56 shows the results of setting the threshold voltages at each frequency to obtain fractional counts of 0.25 for all four bit patterns. The plot shows both the three threshold voltages and the fractional counts. Variation in the fractional counts in Figure 56(b) is due to the simple threshold setting algorithm, which searches for the correct fractional counts in steps of 10mV, and terminates when close enough. Note how the minus threshold voltage is close to, or exceeds the zero threshold for some frequencies. This is due to internal offsets within the digitizer (the threshold setting algorithm did not terminate for \( V_{\text{minus}} > V_{\text{zero}} \) for this test). For both tests, the digitizer clock frequency was 1024MHz, so frequencies above 512MHz are aliased.
Figure 56: Threshold voltages versus frequency for a sinusoidal input. The thresholds are set at each frequency to obtain fractional counts of 0.25 for all four bit patterns. (a) shows the threshold voltages for frequencies from 10MHz to 1020MHz in 10MHz steps. (b) shows the fractional counts recorded at each frequency (ideally all 0.25). Variation in the fractional counts is due to the simple threshold setting algorithm, which searches for the correct fractional counts in steps of 10mV, and terminates when close enough. Note how the minus threshold voltage is close to, or exceeds the zero threshold for some frequencies. This is due to internal offsets within the digitizer. The digitizer clock frequency was 1024MHz, so frequencies above 512MHz are aliased.
13.4 Auto-correlation tests

Figures 57, 58, and 59 show autocorrelations of 16MHz/1008MHz, 128MHz/896MHz, and 256MHz/768MHz sinusoidal signals. The digitizer clock rate for these tests was 1024MHz, so the second frequency measured in each test aliases to the same frequency as the first test, e.g. 1008MHz aliases to 1024MHz-1008MHz = 16MHz. The tests at higher frequencies show slight losses in correlation, probably due to noise (jitter) in the signal source and test setup. The sinusoidal test were performed with the fractional counts all set to 0.25. The lags were normalized by the expected value of the zeroth lag for the 2-bit deleted inner product multiplication scheme used in the correlator; i.e., \((9P_{10} + 9P_{01}) = 2 \times 0.25 \times 9 = 4.5\).

Figures 60, 61, 62, 63, and 64 show the results of noise source autocorrelations. The fractional counts for the bits patterns 10, 11, 00, and 01 were set to 0.18, 0.32, 0.32, and 0.18 respectively. The lags were normalized by the expected value of the zeroth lag; i.e., \((9P_{10} + 9P_{01}) = 2 \times 0.18 \times 9 = 3.24\).

For a signal with a uniform spectrum from dc to \(B\), the lag domain signal is a sinc function. If the sinc function is normalized to unity in the lag domain, then the Fourier transform pair is

\[
sinc(2Bt) \leftrightarrow \frac{1}{2B} \cdot \text{rect} \left( \frac{f}{2B} \right)
\]

Calculation of the Fourier transform using the discrete Fourier transform, or Fast Fourier transform (FFT) introduces some scaling factors in the Fourier domain result; that is,

- time limiting the waveform to period \(T\) introduces a scale factor \(T\)
- the implied periodicity in the time domain of the discrete transforms introduces a scale factor \(1/T\)
- sampling in the time domain every \(\Delta t = 1/f_s\) introduces a scale factor \(f_s\)

Brigham, 1988 contains a clear description of the origin of these scale factors [3]. The result of these scale factors is that the discrete Fourier transform is related to the Fourier transform via

\[
H(f) \approx \frac{1}{f_s} H[n].
\]

Hence, the expected magnitude of the FFT of the autocorrelation lags is

\[
H[n] \approx \frac{f_s}{2B} \cdot \text{rect} \left( \frac{f}{2B} \right)
\]

Figure 60 shows the lags and spectrum from a 128MHz noise source (the is the test noise source from the old OVRO correlator system). With a 1024MHz digitizer clock, the expected, and observed, spectral magnitude of the FFT is 10 log\(_{10}\)(\(f_s/2B\)) \approx 6.0dB. Figure 61 shows the lags and spectrum from a 250MHz low-pass filtered noise source, and the following tests, is a cascade of ZFL-2000 amplifiers providing gain to the thermal noise of a 50Ω termination. The expected spectral magnitude of the 250MHz low-pass spectrum is 3.1dB. Figure 62 shows the lags and spectra from a 500MHz low-pass filtered noise source, along with the expected spectral magnitude of 0.1dB. Figure 63 shows the lags and spectra from a 675MHz to 199MHz band, bandpass filtered noise source. The band aliases to 349MHz to 199MHz (i.e., higher frequencies in the filter alias to lower frequencies). The expected spectral magnitude of the aliased 150MHz band is 5.3dB. Figure 64 shows the lags and spectra from the LORCH 500MHz to 1000MHz, bandpass filtered noise source. This filter is to be used in the continuum correlator downconverter. The expected spectral magnitude is 0.1dB. Because this test was performed with a 1024MHz clock, there is some coherent aliasing at the top end of the spectrum. Figure 65 shows the spectrum measured when using a 1000MHz digitizer clock.
The digitizer evaluation board buffers the input to the SPT7610 digitizer using a Mini-circuits ERA-6SM dc to 4GHz RF amplifier [16]. Figure 66 shows the lags and spectrum of the LORCH filtered noise source without the RF amplifier. The spectrum shows a sinusoidal variation due to frequency dependent VSWR (this variation is also visible as a spike in the lags close to lag zero). There is also some clock noise at 256MHz visible in the spectrum. The use of the RF amplifier on the input to the digitizer evaluation board ensures that the input appears as a 50Ω load to the source driving it. The final digitizer boards should make allowance for a 3dB pad at the input to the RF amplifier, since a pad can be used to improve VSWR further still.

The lags measured for the tests in this section are autocorrelation lags. Since an autocorrelation is symmetric about the lag delay axis, the measurement of lags 0 to \( N - 1 \) provides information on both positive and negative lags. A modified version of the FFT can be used to process real-symmetric data when efficiency is desired (for example in the DSP code), however, for these tests the lags were placed into a symmetric matrix, i.e., \( s = [d(N:-1:1) \ d(2:N) \ 0] \), where \( s \) is a symmetric version of the measure lags \( d \) (in MATLAB matrix format). This data is then FFTed using MATLAB and the positive frequency components are displayed in the figures. For these tests, there was no quantization correction applied to the lags prior to the FFT (for a 1-bit correlator this is also known as the Van Vleck correction). This results in a slightly larger variance in the spectral data that was not of concern for these tests. The data was measured for an integration time of 6.18ms (a phase switch period in the final system). The test setup used a 16 lag correlator and a digital delay line to measure 1024 lags.

A sinusoidal frequency source can be used to obtain information on the bandpass shape of the filters used in a correlator system. The use of a known-frequency sinusoidal source eliminates the problem of aliasing of the signal as was seen in the noise source spectra. Figures 67, 68, 69, and 70 show the response of the zeroth lag of the correlator for varying sinusoidal frequencies, where the output of the frequency synthesizer is filtered by the low-pass or bandpass filters used in the noise source tests. The top plots in each figure contain three lines; the solid line is the zeroth lag response of the correlator, the dashed line is the zeroth lag as calculated from quantization state counters 10 and 01 (2-bit multiplication with deleted inner products), and the dotted line is zeroth lag as calculated from all four quantization state counters (full 2-bit multiplication). The zeroth lag estimate for full 2-bit multiplication drops from 5 to 1 when the sinusoid amplitude drops below the threshold voltages, so the normalized zeroth lag estimate has a minimum of \( 10\log_{10}(1/5) = -7.0 \text{dB} \). The zeroth lag estimate for the deleted inner product estimates drops to zero once the sinusoid amplitude drops below the threshold voltages. It should be emphasized that these plots do not display spectra, they display the loss in the estimate of the zeroth lag. Variation of the lag zero response within the bandpass of the filter is due to the variations in offset voltages as seen by the plus and minus threshold voltages, this variation can be seen in the fractional count plots shown in each figure. The fractional count plots should be compared to Figure 55, which contains the fractional counts without an input filter. Figure 71 compares the filter response as measured using a network analyzer, with the zero lag response from Figure 70. The zero lag response shows a much faster drop in response near the band edges, hence the zero lag response should not be used to infer the filter response.
Figure 57: 16MHz/1008MHz lags.

Figure 58: 128MHz/896MHz lags.
Figure 59: 256MHz/768MHz lags.

Figure 60: 128MHz noise source lags/spectrum.
Figure 61: 250MHz low-pass filtered noise source lags/spectrum.

Figure 62: 500MHz low-pass filtered noise source lags/spectrum.
Figure 63: 675MHz to 825MHz band-pass filtered noise source lags/spectrum.

Figure 64: 510MHz to 980MHz (745MHz center/470MHz bandwidth) LORCH band-pass filtered noise source lags/spectrum. 1024MHz digitizer clock generated using a PLL and 16MHz crystal reference.
Figure 65: LORCH band-pass filtered noise source lags/spectrum. 1000MHz digitizer clock generated using a PLL and 15.625MHz reference from a frequency synthesizer. The additional noise in the spectrum relative to Figure 64 is due to the synthesizer.

Figure 66: LORCH band-pass filtered noise source lags/spectrum. 1024MHz digitizer clock generated using a PLL and 16MHz crystal reference. This data was recorded with a direct connection to the digitizer input, i.e., the RF amplifier on the digitizer evaluation board was bypassed.
Figure 67: 250MHz low-pass filter zero lag and fractional count response.

Figure 68: 500MHz low-pass filter zero lag and fractional count response.
Figure 69: 675MHz to 825MHz band-pass filter zero lag and fractional count response.

Figure 70: 510MHz to 980MHz (745MHz center/470MHz bandwidth) LORCH band-pass filter zero lag and fractional count response.
Cross-correlation tests use two digitizer evaluation boards chained on the same parallel port (EPP mode). Each digitizer evaluation board system controller will respond to a 7-bit address range. The MSB of the 8-bit address from the parallel port is used as a board select. The header located on the digitizer indicates whether a particular board should respond to addresses in the range 0x00 to 0x7F (header loaded), or 0x80 to 0xFF (header open).

The correlator board FPGA HDL for processing cross-correlations requires that FPGA0 and FPGA1 be configured as digitizer FPGAs, and that their digital delay line output data be routed to a correlator FPGA (for cross-correlation). The results of cross-correlator testing can be found in the correlator board test results documentation.
References


