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LVDS Fanout Board Description:

The fanout board receives data from a digitizer board. The received LVDS data is terminated, converted to LVCMOS and transmitted along a multi-drop 3.3V LVCMOS bus. The data is then converted to LVDS for transmission to correlator boards. Each transmitter block drives the LVDS signals onto two VHDCI connectors. Note that there are no LVDS transmitter terminations. If a single LVDS cable is attached, then the transmitters will be driving an end-terminated LVDS bus. If two LVDS cables are attached, then the transmitters will be center driving a bus terminated at each end.

Power consumption:

4 ICs configured as Receivers with ICCR = 80mA (max)
12 ICs configured as Drivers with ICCD = 80mA (max)
Total transceiver current 16 x 80mA = 1.28 A
LVCMOS termination current = 33 x 13mA = 429mA
Total current 1.28A + 0.43A = 1.71A
Total power at 3.3V = 5.6W
DECOUPLING REQUIREMENTS:

SINCE THE 4 LVDS TRANSEIVERS ARE LOCATED VERY CLOSE TOGETHER AND ARE ON BOTH SIDES OF THE BOARD, NOT ALL DECOUPLING CAPS WILL BE NECESSARY. PLEASE PLACE AS MANY AS POSSIBLE. USE PAT TRACES TO DECOUPLING CAPS.
DECOUPLING REQUIREMENTS:
SINCE THE 4 LVDS TRANSCIEVERS ARE LOCATED VERY CLOSE TOGETHER AND ARE ON BOTH SIDES OF THE BOARD, NOT ALL DECOUPLING CAPS WILL BE NECESSARY. PLEASE PLACE AS MANY AS POSSIBLE. USE FATTY TRACES TO DECOUPLING CAPS.

TRANSMITTER BLOCK NUMBER: 1

THIS PART IS PLACED ON THE TOP SIDE OF THE PCB

THIS PART IS PLACED ON THE BOTTOM SIDE OF THE PCB
DECOUPLING REQUIREMENTS:

SINCE THE 4 LVDS TRANSCIVERS ARE LOCATED VERY CLOSE TOGETHER AND ARE ON BOTH SIDES OF THE BOARD, NOT ALL DECOUPLING CAPS WILL BE NECESSARY. PLEASE PLACE AS MANY AS POSSIBLE. USE FAT TRACES TO DECOUPLING CAPS.

TRANSMITTER MODE

Transmitted LVDS Clock and Data

LDDATA[31..0]
LDDATA[30..15]
LDDATA[14..0]
LDDATA[15..0]

LVCMOS Clock and Data

DATA[31..0]
DATA[30..15]
DATA[14..0]
DATA[15..0]
CLK
TRANSMITTER BLOCK NUMBER: 3

DECOUPLING REQUIREMENTS:

SINCE THE 4 LVDS TRANSCEIVERS ARE LOCATED VERY CLOSE TOGETHER AND ARE ON BOTH SIDES OF THE BOARD, NOT ALL DECOUPLING CAPS WILL BE NECESSARY. PLEASE PLACE AS MANY AS POSSIBLE. USE FAT TRACES TO DECOUPLING CAPS.

This part is placed on the top side of the PCB.

This part is placed on the bottom side of the PCB.

Transmitted LVDS Clock and Data

LVCMOS Clock and Data

LVDS DE

LVDS RE#
Termination values assume 60-Ohm transmission lines.

(65-Ohms was not used as 130-Ohm termination packs were not available)

3.3V / 240-Ohm = 13.75mA, so 33 terminations consume 454mA
CPCI Connector J1

Power Filter LVDS Transceiver

BULK DECOUPLING FOR VCC3

2A-rated EMI Filter

LVDS Transceiver power filtering

CHASSIS GROUND (ALONG THE EDGES OF THE CARDS AND THE CONNECTOR SHIELDS) IS TIED TO LOGIC GROUND (GND) AS OFTEN AS POSSIBLE ALONG THE PERIPHERAL OF THE BOARD.

PLACE AS MANY AS POSSIBLE

GND CHASSIS GND

Chassis-to-logic ground coupling